HIGH PERFORMANCE ORGANIC THIN-FILM TRANSISTOR WITH SPECIAL OXIDE CONTACT STRUCTURE AND EVALUATION OF DEVICE PHYSICS

Final Thesis Submitted

By

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For

The Partial Fulfillment of the Degree of

Doctor of Philosophy

(Ph. D)

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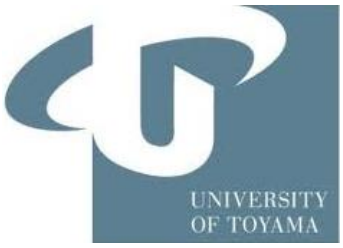

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July 2013

ACKNOWLEDGEMENTS

This thesis is the result of not only my efforts but also those of others who have supported me in different ways all along my Ph.D. program.

First of all, I thank Allah, the almighty, for giving me the strength to carry on my study and for blessing me with many great people who have been my greatest support in both my personal and professional life. With heartfelt gratitude, first I would like to seize this opportunity to express my deepest regards, gratitude and sincere thanks to my supervisor Prof. Hiroyuki Okada for his dedication, sincere effort and guidance from the early stage of this research as well as giving me extraordinary experiences throughout the work. I am very thankful for his valuable time, guidance and giving me chance to work in such a reputed institution. His passion and dedication to phonology has a strong effect on his students including me. He is very patient, understanding and above all a very good human being. I was really lucky and blessed to be taught by such a phenomenal teacher who truly believes in the power of education in positively shaping and changing peoples' lives to the best and I am very much honored to work under his esteemed guidance.

I am also very thankful to Prof. Shigeki Naka for dedicating much of his time to help me with many of the problems I faced while conducting the study and experiments.

I especially thank to Mr. Miki Shibata for the great help in many experiments.

I have no words to express my feeling for my family, whose love and constant encouragements have helped me to complete this journey. My family was also a huge part of my life. Thus,

acknowledging them will be the least of what I can do to show my appreciation. I would like to give special thanks my brother Dr. Ahsanulhaq Qureshi and Tanveer Ahmed Mir for their love and constant moral support, which guided me through this project. Their patience and sacrifice are always a main source of my inspiration and will remain throughout my life motivating me to pursue still higher goals.

Finally, heartfelt thanks to all my friends, colleagues and other lab member for their unfailing help, constant encouragement and timely help right from introducing me to the laboratory to teaching me various experimental techniques till the end of my project.

Finally I would like to give Special thanks to all the referees for my Ph. d Course and other staff members of University of Toyama for all kind of helps throughout my study.

Mir Waqas Alam

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Abstract

Organic thin-film transistors (OTFTs) have attracted increasing interest for their potential advantages, such as, low cost, lightweight and possible fabricating on flexible substrate, as well as large-area feasibility. For constructing a high performance top-contact OTFT, it is very important to understand the influence of interfaces, which play a crucial role in the overall performance of the device. Mainly there are two kinds of interfaces in the OTFT. First is in between the semiconductor and the gate dielectric, where the conducting channel forms. The second one is in between the source/drain (S/D) electrodes and the semiconductor layer where charge carriers are injected.

First, I particularly discussed the latter interface. Organic and metal interfaces mostly limit the performance of the device and field effect mobility is also decreased. In earlier reports it has been shown that the diffusion between the metal electrode and pentacene reduce the hole injection carrier at the interface which causes the increase in barrier height and contact resistance which effect the performance of the OTFTs. It is shown that the contact between the S/D electrodes and the organic semiconductor can be improved by inserting transition metal oxide layer as carrier injection layers. Because of good electronic properties, transition metal oxides such as molybdenum oxide (MoO_3), tungsten oxide (WO_3) and vanadium oxide (V_2O_5), and other oxides such as germanium oxide (GeO), titanium oxide (TiO_2) offer a unique opportunity to control the work function, and hence increase the charge-injection properties. Therefore, by modifying the organic/electrode interface, the S/D electrodes do not directly contact with pentacene layer and hence significantly reduces the contact resistance, barrier height and

provides protection from diffusion and other chemical reactions, which increase device performance.

Second, I investigated that the enhancement of the charge injection and field effect mobility by inserting a thin (5 nm) MoO_3, GeO, WO_3 and TiO_2 interlayer between the Au electrode and pentacene layer in a top contact pentacene based organic thin-film transistor (OTFTs).In comparison with the pentacene-based OTFT with only-Au electrode, the device performance with bilayer electrode has been considerably improved. The device performance including field effect mobility, threshold voltage, and On/Off ratio of all the device after modification was highly improved, and the highest mobility of 0.96 $cm^2V^{-1}s^{-1}$, threshold voltage of -4 V, and highest on/off ratio of 5.2×10^4 were achieved in the device with 5 nm GeO. I further investigated the temperature dependence of I_D–V_D characteristics which showed strong temperature dependence in all the devices.

Third, the obvious temperature dependence of I_D-V_D curves in all devices suggests that the charge injection characteristics can be fitted by the Schottky emission mechanism. By plotting the relationship between $ln(I)$ vs $V^{1/2}$ and extrapolating straight lines to the ordinal point, the current at zero voltage I_0 is determined. By using the values of I_0, the relationship between $ln(I_0/T^2)$ vs $1/T$ is plotted and from the resulting slope of extrapolated lines. While in case of bilayer MoO_3/Au shows 0.03 eV, WO_3/Au shows 0.05 eV, TiO_2/Au showed 0.04 eV and with only Au electrodes barrier height of 0.12 eV is achieved. The lowest barrier heights of 0.01 eV could be achieved in case of bilayer GeO/Au electrodes. It is assumed that the barrier height was dramatically reduced by inserting thin oxide layer between the Au and pentacene layer.

Similarly, from surface morphology of pentacene, the root mean square roughness is also decreased after inserting metal oxide layer. The main factor for the improvement in the performance of the OTFTs with bilayer electrodes was explained in terms of the reduction in barrier height and smoothed surface roughness of active layer. Therefore, the combination of a thin oxide layer with Au as a bi-layer electrode is an effective way to improve the characteristics of OTFTs, which makes the device suitable for commercial applications.

Finally, I further reported the enhanced carrier injection in pentacene OTFTs with a thin MoO_3-doped pentacene layer between pentacene semiconductor and the S/D electrodes. Device performance including drain current, field effect mobility, and threshed voltage are improved by employing a MoO_3-doped pentacene thin layer. The barrier height at the Au/pentacene interface is lowered from 0.12 to 0.05 eV after inserting a MoO_3-doped pentacene thin layer between them.

Chapter 1

General Introduction and Progress in OTFTs

In Chapter 1 we give the general introduction of organic devices and organic thin-film transistors (OTFTs). The progress in the development of OTFTs, comparison with inorganic transistors and application of OTFTs is also reviewed. At the end of this chapter the motivation and organization of the thesis is also mentioned.

1.1 General Introduction

From last few decades, Organic electronics has been the focus of study and playing a significant role into the commercial world and it seems if the field continues to progress at its current rapid pace, electronics based on organic materials will become a mainstay of our technological existence. More recently, organic electronic and optical phenomena have been the domain of pure research. The main reason for the attraction of this field has been the ability to modify chemical structure during deposition in thin film in such ways which could directly impact the properties of the materials. The use of organic compounds in electronic applications has known a spectacular evolution. Organic semiconductors are promising materials because of a few special properties. Mechanical flexibility of organic materials is an important feature for some future products such as roll able displays and wearable electronics [1, 2]. Also, low capital cost methods of depositing organic material, such as printing and casting should enable production of electronics at ultra-low cost and over very large areas (much larger than silicon wafers). These production methods make organic electronics good candidates for producing very

cheap radio frequency identification (RFID) tags and very large-area electronic displays [3]. The chemical and electrical tune abilities of organic compounds allow the design of various chemical sensors and optical devices [4, 5]. In particular, the development of organic thin-film transistors (OTFTôs), light-emitting diodes (OLEDs), solar cells and photovoltaic cells has attracted a great deal of interest [6-9]. Such interesting properties of organic semiconductors have attracted a lot of attention all around the world. As a result the organic electronic industries had very rapid growth in the last few decades.

A number of different organic materials have been introduced in organic devices. The organic materials used in electronic and optoelectronic devices are generally split into two groups i.e., small molecules and polymers. The former are typically deposited by vapor methods in low or high vacuum environments and have a well-defined molecular weight. Polymers, on the other hand, must be processed from solution and have a molecular weight distribution that is described by the poly dispersity of the materials, giving polymers good glass-forming and mechanical properties. The use of organic compounds as active materials in electronic and optoelectronic devices opens the door to a large number of efficient and potentially low-cost methods for fabricating useful and complicated structures that are inaccessible by conventional methods using conventional semiconductors. For example, the techniques available for processing and patterning organic materials move far beyond the lithographic methods that govern inorganic devices. Organic semiconductors form the basis for a wide range of electronic devices that utilize their high speed and small size for integration on a massive scale. Organic devices have the ability to have a great impact. However, they will not compete directly with silicon or gallium arsenide due to the lower charge mobilityôs and device lifetimes of organic based systems.

Nevertheless, organic devices and circuits are technologically interesting because they have potential to serve in inexpensive and flexible electronic circuits.

1.2 Progress in OTFTs

Pioneering work on OTFTs started in 1983 by Ebisawa using polyacetylene as anactive semiconductor [10]. A few years later in 1986, Tsumura demonstrated an OTFTs with polythiophene in which a large modulated current was obtained [11]. Then, OTFTs using poly (3-hexylthiophene) as an active semiconductor were reported in 1988 [12]. Most of these early OTFTs were fabricated using thin films of polymeric semiconductors formed from solution by spin coating, screen printing or inject printing. The polymer films are typically amorphous, and the carrier mobility is rather low, ranging from 10-5 to10-4 cm2/Vs. In contrast, small-molecule semiconductors can be deposited from a gas phase by vacuum thermal evaporation or by organic vapor phase deposition and the molecules can pack into well-organized polycrystalline films, which leads to higher carrier mobility. Another advantage of small molecules is that their charge transport can be controlled by modifying various molecular parameters and deposition conditions. In 1989, Horowitz *et al*. demonstrated the first OTFT using a small-molecule semiconductors exithiophene [13] with higher carrier mobility of 10^{-3} cm^2/Vs and on/off current ratio of 10^5. Pentacene, the most important small-molecule semiconductors so far, was applied to OTFTs in 1991 [14, 15]. By 1997, the pentacene OTFTs had achieved a high carrier mobility of 1.5 cm^2/Vs and an on/off current ratio of 10^8, which are comparable with the electronic performance of hydrogenated Si TFTs [16]. Later on in 2003, 3M reported pentacene OTFTs with a field-effect mobility value up to 7 cm^2/Vs [17]. However, most groups can only routinely obtain mobility

around 1cm^2/Vs with thin-film pentacene. All the semiconductors mentioned above are *p*-type in which the conduction in the materials is due to the positively charged carriers. However, in order to realize applications such as organic complementary logic circuits [18], both *p*-type and *n*-type organic semiconductors are needed with comparable electrical performance. A small number of *n*-type organic materials in which the conduction is due to the negatively charged carriers have been investigated, including fullerene C60 (buckminsterfullerene or buck balls) [19,20], fluorocarbon-substituted thiophene oligomers [21-23], naphthaleneandperylene derivatives [24-26], etc. Among these *n*-type organic semiconductors, C60 holds promise for high-mobility *n*-type OTFTs since Haddon [19] first reported it in1995. Electron mobilityôs as high as 4.9 cm^2/Vs and 6 cm^2/Vs have been reported by Itaka [27] and Anthopoulos [28], both using C60 as active materials. However, the on/off current ratio in the former was inevitably reduced with pentacene (a well-known *p*-type semiconductor) at the dielectric/semiconductor interface. In the latter report, C60 was deposited by hot wall epitaxy (HWE) requiring undesirably high deposition temperatures up to 250 ºC. On the other hand, the issue with high threshold voltage in *n*-type OTFTs, which greatly hinders its application in circuit operation, has not been addressed in both cases.

1.3 OTFTs vs. Inorganic Thin-Film Transistors

OTFTs, thin-film transistors (TFTs) with organic semiconductors as the active layers, are of great interest as a potential alternative to amorphous Si TFTs. With remarkable progress in the synthesis and purification of organic semiconductors and the processing of these materials into devices, the mobility of the best OTFTs has surpassed that of Si TFTs [29]. A major advantage

of OTFTs vs. Si TFTs is their compatibility with low-cost, low-temperature processes. A typical Si: H TFT fabrication process involves the deposition of hydrogenated Si as an active layer and silicon nitride as a gate dielectric by plasma enhanced chemical vapor deposition (PECVD) using H_2/SiH_4 (silane) and NH_3/SiH_4, respectively. The process temperature is usually much higher than 250 °C, which enables the use of inexpensive glass as substrate [30]. However, this fabrication process is not compatible with colorless, transparent flexible polymeric substrate materials, which typically require a temperature below 200 ºC. OTFTs, on other hand, can be processed at much lower temperatures using various simple, low cost techniques, including vacuum thermal evaporation, spin-coating, dip-coating, vapor deposition, micro contact printing, screen-printing, etc. The combination of low-temperature processibility with the mechanical flexibility of organic materials thus leads to a wide range of applications in flexible electronics with a potential for very low cost manufacturing. Secondly, Si technology provides only high performance *n*-channel transport which prevents the use of complementary metal-oxideï semiconductor (CMOS) technologies. In contrast, the versatility of synthetic organic chemistry has enabled the tailoring and engineering of both *n*- and *p*-type semiconductors, giving rise to many potential candidates for circuit designs based on CMOS technology.

1.4 Application of OTFTs

The earliest applications of organic optoelectronic devices were the solar cells and organic thin-film transistors (OTFTs). Inorganic based solar cells and transistors were well developed and are being deployed worldwide however the high cost of their manufacture ultimately limits their widespread acceptance as a source of renewable energy. The devices based on organic materials

can be potentially fabricated by simple and easy techniques, not requiring the demanding environment needed for inorganic based devices. The potential for low-cost manufacturing afforded by organic devices gives organic solar cells the potential to significantly impact the energy landscape, making them useful in a wide range of environments. In their contribution, chemical sensing is also emerging as an important application for organic materials. Uses in military, biomedical, and industrial environments are ubiquitous, and having the ability to sensitively detect specific chemicals, both accurately and inexpensively, could vastly expand their applications. Research on advanced organic materials has led to marked improvements in the sensitivity and versatility of chemical sensors.

Organic and polymer transistor based circuits are being investigated for a number of low-cost, large-area applications, particularly those that are compatible with flexible plastic circuit [31-35]. The organic materials that have been used as active semiconductor materials include both sublimed and solution-processed semiconductors such as pentacene, oligothiophenes, hexadecafluorocopper, phthalocyanine, polythiophene, etc. This choice of materials opens up several possibilities to develop integrated circuit technologies based on organic transistors for various large-area, low-cost applications. Organic thin-film transistors (OTFTs) have been proposed for applications such as display switches [36], display drivers [37, 38], radio-frequency identification (RFID) tags [39-41], and sensors [42-43]. OTFTs that are solution processable and comprise excellent device properties are key requirements in their successful realisation into large area electronics such as active matrix displays as well as into low-cost electronic devices such as radio frequency electronic tags. Organic/polymer transistors have also been integrated with optical devices such as light-emitting diodes (LEDs), electrophoretic cells, and liquid

crystals. In recent years, the complexity of circuits made with organic transistors has increased, and the first large-scale (864 transistor) complementary circuits have been fabricated. Researchers have reported active-matrix displays and electronic paper with hundreds or thousands of transistors. The speed of ring oscillators is now in excess of 100 kHz and the clock speed of clocked sequential circuits such as registers is in the kilohertz range. There is a need to develop technologies for relatively fast circuits (~100 kHz clock rate) for use in RFID tags and display drivers. One way to accomplish this is with a complementary technology combing pentacene p-channel transistors with and n-channel technology utilizing materials with electron mobility in excess of 0.1 cm^2/Vs. There have been a few such materials reported in recent years, with many more currently being synthesized [44-48].

In addition to the applications reviewed above, organic transistors have been proposed for other applications. Since the first reports of integrated OLEDs and transistors, there have been advances in the performance of both organic/polymer LEDs and transistors. This has led to increased research activity in designing organic FET-based pixel electronics for active-matrix OLED displays. Light emission from an organic transistor has been proposed and subsequently observed by several groups. This promises to be an interesting area of device research in terms of both the materials that need to be developed for efficient light emission and transport, and the device design challenges and opportunities that exist. Another applications area that appears promising is the use of OTFTs in large-area sensor and detector circuits. Along these lines, it is anticipated that new and innovative applications that take advantage of the unique properties of organic and polymer transistors will continue to appear, providing added impetus for advances in both materials and processing development.

1.5 Motivation and Organization of the Thesis

The primary objective present study is to develop the high-performance OTFTs, with special oxide contact structure through interface engineering at the interface between the organic semiconductor and the source/drain electrodes. In current research Pentacene a widely used, commercially available semiconductor is used a active layer and Gold (Au) is used as the Source/Drain electrode. The mismatch between the HOMO level of pentacene and the work function of Au results to relatively high injection barrier and contact resistance at the Pentacene/Au interfaces which mostly limit the electrical performance of the device. Because of good electronic properties, transition metal oxides such as molybdenum oxide (MoO_3), tungsten oxide (WO_3) and vanadium oxide (V_2O_5), and other oxides such as germanium oxide (GeO), titanium oxide (TiO_2) offer a unique opportunity to control the work function, and hence increase the charge-injection properties. We modify the organic/electrode interface, by introducing above mention metal oxides layer between S/D electrode so that the S/D electrodes do not directly contact with pentacene layer and hence significantly reduces the contact resistance, barrier height and provides protection from diffusion and other chemical reactions, which increase device performance. The following aspects are investigated: first, the surface morphology including root mean square roughness of pentacene layer secondly, the barrier height and energy level alignment between S/D electrodes and the organic semiconductor.

Through device engineering with an optimized interface at the Pentacene/Au high-performance OTFTs were realized with excellent device characteristics including a high mobility, a low threshold voltage, a low sub threshold slope, and a high on/off current ratio.

According to the motivations and objectives outlined above, the organization of the dissertation is structured as follows. Chapter 1 reviews the basic background of organic semiconductors and organic thin film transistors (OTFTs). The progress in the development of OTFTs, comparison with Si-based transistors and application of OTFTs were briefly discussed.

Chapter 2, provides a detailed description of experimental methods used in this dissertation work. It starts with the illustration of device structures and operation, followed by the electrical characterization of OTFTs. Four common device structures used in transistors are compared and different source/drain arrangements are explained. The operation of OTFTs with a p-type semiconductor is systematically analyzed and illustrated. The current-voltage characteristics and the extraction of electrical performance in the linear and saturation regimes for OTFTs are explained. The critical steps involved in the OTFT fabrication Such as semiconductors deposition, preparation of gate dielectrics, and deposition of metal contacts and theoretical concept of dielectric layer and organic semiconductors are also included.

In Chapter 3, we will discuss the details of charge injection and organic/metal contact in organic thin film transistors. Interface properties of the metal/semiconductor and insulator/semiconductor have a strong influence on the device performance. Optimization of the interface between the source/drain (S/D) electrode and the organic semiconductor is one of the important factors for the organic thin film transistor (OTFTs) performance along with the insulatorï semiconductor interface.

Later, the main results of our study will be included in which one by one all published paper will be discussed.

1.6 References

[1] J. A. Rogers and Z. Bao: Poly. Chem. **40**, 3327, 2002.

[2] A. Bonfiglio, D. De Rossi, T. Kirstein, I. R. Locher, F. Mameli, R. Paradiso, and G. Vozzi, IEEE Transactions on Information Technology in Biomedicine, **9**, 319, 2005.

[3] R. Bansal: Antennas and Propagation, Magazine, IEEE, **45**, 105, 2003.

[4] B. Crone, A. Dodabalapur, A. Gelperin, L. Torsi, H. E. Katz, A. J. Lovinger and Z. Bao: Appl. Phys. Lett. **78**, 2229, 2001.

[5] E. Berkovich, J. Klein, T. Sheradsky, E. R. Silcoff, K. T. Ranjit, I. Willner, G. Nakhmanovich, V. Gorelik and Y. Eichen: Syn. Met.**107**, 85, 1999.

[6] S. R. Forrest: Chem. Rev. **97**, 1793, 1997.

[7] C. W. Tang and S. A.van Slyke: Appl. Phys. Lett. **51**, 913, 1987.

[8] C. W. Tang: Appl. Phys. Lett. **48**, 183, 1986.

[9] D. Braga and G. Horowitz: Adv. Mat. **21**, 1473, 2009.

[10] F. Ebisawa, T. Kurokawa and S. Nara, J. Appl. Phys. **54**, 3255, 1983.

[11] A. Tsumura, H. Koezuka and T. Ando: Appl. Phys. Lett. **49**, 1210, 1986.

[12] A. Assadi, C. Svensson, M. Willander and O. Inganas: Appl. Phys. Lett. **53**, 195, 1988.

[13] G. Horowitz, Solid State Commun. 72, 381, 1989.

[14] G. Horowitz, X. Peng, D. Fichou and F. Garnier: Journal of Mol. Elec. **7**, 85, 1991.

[15] G. Horowitz, D. Fichou, X. Peng and F. Garnier: Syn. Met. **41**, 1127 1991.

[16] D. J. Gundlach, Y. Y. Lin, T. N. Jackson, S. F. Nelson and D. G. Schlom: IEEE Elec. Dev. Lett. 1**8**, 87, 1997.

[17] T. W. Kelley, D. V. Muyres, F. P. Baude, T. P. Smith and T. D. Jones: Mat. Res. Soc. San

Francisco, CA, United States, **771**, 169, 2003.

[18] T. Kanbara, K. Shibata, S. Fujiki, Y. Kubozono, S. Kashino, T. Urisu, M. Sakai, A. Fujiwara, R. Kumashiro and K. Tanigaki: Chem. Phy. Lett. **379**, 223, 2003.

[19] R. C. Haddon, A. S. Perel, R. C. Morris, T. T. M. Palstra, A. F. Hebard and R. M. Fleming: Appl. Phys. Lett. **67**, 121, 1995

[20] M. Kitamura, Y. Kuzumoto, M. Kamura, S. Aomori and Y. Arakawa: Appl. Phys. Lett. **91**, 183514, 2007.

[21] A. Facchetti, M. Mushrush, H. E. Katz and T. J. Marks: Adv. Mat. **15**, 33, 2003.

[22] M.-H. Yoon, S. A. D. Benedetto, A. Facchetti and T. J. Marks: Journal of the American Chem. Soc. **127**, 1348, 2005.

[23] R. J. Chesterfield, C. R. Newman, T. M. Pappenfus, P. C. Ewbank, M. H. Haukaas, K. R. Mann, L. L. Miller and C. D. Frisbie: Adv. Mat. **15**, 1278, 2003.

[24] P. R. L. Malenfant, C. D. Dimitrakopoulos, J. D. Gelorme, L. L. Kosbar, T. O. Graham, A. Curioni and W. Andreoni: Appl. Phys. Lett. **80**, 2517, 2002.

[25] R. J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. A. Da Silva Filho, J.-L. Bredas, L. L. Miller, K. R. Mann and C. D. Frisbie: J. Phys. Chem. B **108**, 19281, 2004.

[26] M. Ling, P. Erk, M. Gomez, M. Koenemann and J. Locklin: Adv. Mat. **19**, 1123, 2007.

[27] K. Itaka, M. Yamashiro, J. Yamaguchi, M. Haemori, S. Yaginuma, Y. Matsumoto, M. Kondo and H. Koinuma: Adv. Mat. **18**, 1713, 2006.

[28] T. D. Anthopoulos, B. Singh, N. Marjanovic, N. S. Sariciftci, A. Montaigne Ramil, H. Sitter, M. Colle and D. M. de Leeuw: Appl. Phys. Lett. **89**, 213504, 2006.

[29] T. W. Kelley, L. D. Boardman, T. D. Dunbar, D. V. Muyres, M. J. Pellerite and T. P. Smith:

Journal of Phy. Chem. B **107**, 5877, 2003.

[30] C. R. Kagan and P. Andry, Thin-Film Transistors, 1st ed. Boca Raton, FL, USA: CRC Press, 2003.

[31] C. J. Drury, C. M. J. Mutsaers, C. M. Hart, M. Matters and D. M. de Leeuw: Appl. Phys. Lett. **73**, 108, 1998.

[32] U. Zschieschang, H. Klauk, M. Halik, G. Schmid and C. Dehm, Adv. Mater. **15**, 1147, 2003.

[33] H. Klauk, M. Halik, U. Zschieschang, F. Eder, G.Schmid and C Dehm: Appl. Phys. Lett. **82**, 4175, 2003.

[34] Z. Bao, Y. Feng , A. Dodabalapur , V. R. Raju and A. J. Lovinger: Chem. Mater. **9**, 1299, 1997.

[35] P. Mach, S. J. Rodriguez, R. Nortrup, P. Wiltzius and J. A. Rogers: Appl. Phys. Lett. **78**, 3592, 2001.

[36] A. Dodabalapur, Z. Bao, A. Makhija, J. G. Laquindanum, V. R. Raju, Y. Feng, H. E. Katz and J. Rogers: Appl. Phys. Lett. **73**, 142, 1998.

[37] H. Sirringhau, N. Tessler and Richard H. Friend: Science **280**, 1741, 1998.

[38] T. N. Jackson, Y. Y. Lin, D. J. Gundlach and H. Klauk: IEEE J. Sel. Top. Quant. Electron.**4**, 100, 1998.

[39] Y. Watanabe and K. Kudo: Appl. Phys. Lett.**87**, 223505, 2005.

[40] C. D. Dimitrakopoulos, and P. R. L. Malenfant: Adv. Mater. **99**, 1144, 2001.

[41] S. Molesa, D. R. Redinger, D. C. Huang and V. Subramanian: Mater. Res. Soc. Symp. Proc. **769**. H8.3, 2003.

[42] B.K. Crone, A. Dodabalapur, A. Gelperin, L. Torsi, H. E. Katz, A. J. Lovinger and Z. Bao:

Appl. Phys. Lett. **78**, 2229, 2001.

[43] B. K. Crone, A. Dodabalapur, R. Sarpeshkar, A. Gelperin, H. E. Katz and Z. Bao: J. Appl. Phys. **91**, 10140, 2002.

[44] H. E. Katz, A. J. Lovinger, J. Johnson, C. Kloc, T. Siegrist, W. Li, Y.-Y. Lin and A. Dodabalapur: Nature **404**, 478, 2000.

[45] R.J. Chesterfield, J. C. McKeen, C. R. Newman, P. C. Ewbank, D. Filho, J.-L. Bredas, L. L. Miller, K. Mann and C.D. Frisbie: J. Phys. Chem. B **108**, 19281, 2004.

[46] B. A. Jones, M. J. Ahrens, M. H. Yoon, A. Facchetti, T. J. Marks and M. R. Wasielewski: Angew. Chem. Int. Ed. **43**, 6363, 2004.

[47] P. R. L. Malenfant, C. D. Dimitrakopoulos, J. D. Gelorme, L. L. Kosbar, T. O. Graham, A. Curioni and W. Andreoni: Appl. Phys. Lett. **80**, 2515, 2002.

[48] S. Kobayashi, T. Takenobu, S. Mori, A. Fujiwara and Y. Iwasa: Appl. Phys. Lett. **82**, 4581, 2003.

Chapter 2

Fabrication and Experimental details of OTFTs

Chapter 2 provides a detailed description of experimental methods used in this dissertation work. It starts device structures and operation, followed by the electrical characterization of OTFTs. The critical steps involved in the OTFTs fabrication Such as semiconductors deposition, preparation of gate dielectrics, deposition of metal contacts and theoretical concept of dielectric layer and organic semiconductors are also included.

2.1 Structure of OTFTs

Transistors as the building blocks of any electronic circuit are the main concern in developing organic electronics. For high performance organic thin film transistors, with application to display and focal plane array backplanes, as well as very low cost logic circuits, the organic material must have high carrier mobility and On/Off ratio. Changes at the molecular level significantly affect all of these parameters, giving the chemist an unprecedented degree of flexibility in materials design.

To make OTFTs, need to have organic semiconductor (OSC), gate, dielectric insulator, contact electrodes and the substrate. Plastic, Silicon and glass substrate were highly used for the fabrication of OTFTs. The gate insulator should be organic to reduce the thermal stress induced by the difference in the thermal expansion coefficient between TFT, organic semiconductor layer and substrate. Many organic semiconductor materials have been analyzed and among them pentacene is highly used. It consists of three electrodes one of these electrodes is called source

while the other drain and the third electrode is called gate. Source and drain gold electrodes are separated by a distance L called the channel length and each other, defining a channel of width W. OTFTs device structures, determined by the position of the contacts (i.e., gate, source, and drain) relative to the organic semiconductor film, are similar to those of inorganic TFTs. The basic structures are either coplanar or staggered. The device cross-sections of the OTFT test configurations are shown in Fig. 2.1.1. They are simplified structures without considering individual device patterning. In a coplanar structure, also called bottom-contact structure, where the gate, source, and drain contacts are all located on the same side of the organic semiconductor film, as shown in Fig..2.1.1 (a) and (c). In bottom-contact structure the source/drain is deposited on an insulating and semiconducting material is deposited on the top of the device. In a staggered structure, also called top-contact structure, the gate contact is on the opposite side of the organic semiconductor film from the source and drain contacts, as shown in Fig.2.1.1 (b) and (d). In top-contact structure the source/drain are deposited on top of the device. Each structure has two different configurations depending on the position of the gate contact, on the bottom side (bottom-gate or inverted) [Fig.2.1.1 (a) and (b)] or the top side (top-gate) [Fig.2.1.1 (c) and (d)] of the organic semiconductor film, respectively. Therefore, there are four basic device configurations based on the definitions above as summarized in Fig.2.1.1: (a) inverted-coplanar structure, (b) inverted-staggered structure, (c) top-gate coplanar structure, and (d) top-gate staggered structure. Top-gate device structures as shown in Fig.2.1.1 (c) and (d) have been applied to fabricate polymer TFTs [1, 2] but have not been widely used in the fabrication of OTFTs. The electrical performance of OTFT devices with a top-gate structure can be significantly degraded during the deposition process of the top

electrodes, and the film growth can be disturbed at the interface of organic semiconductor/metal contacts. The inverted-coplanar device structure as shown in Fig.2.1.1 (a) is often referred as bottom-contact in the OTFT literature and the inverted-staggered device structure shown in Fig.2.1.1 (b) is often referred as top-contact in the OTFT literature. In bottom-contact OTFT devices, the organic semiconductor is deposited onto the gate insulator and source/drain contacts. In top-contact OTFT devices, the source/drain contacts are usually deposited on the organic semiconductor through a shadow mask. To facilitate the evaluation of new organic semiconductor materials, heavily n-doped silicon (*n*++-Si) wafer as the gate contact and thermal SiO_2as gate insulator are used in these two structures.

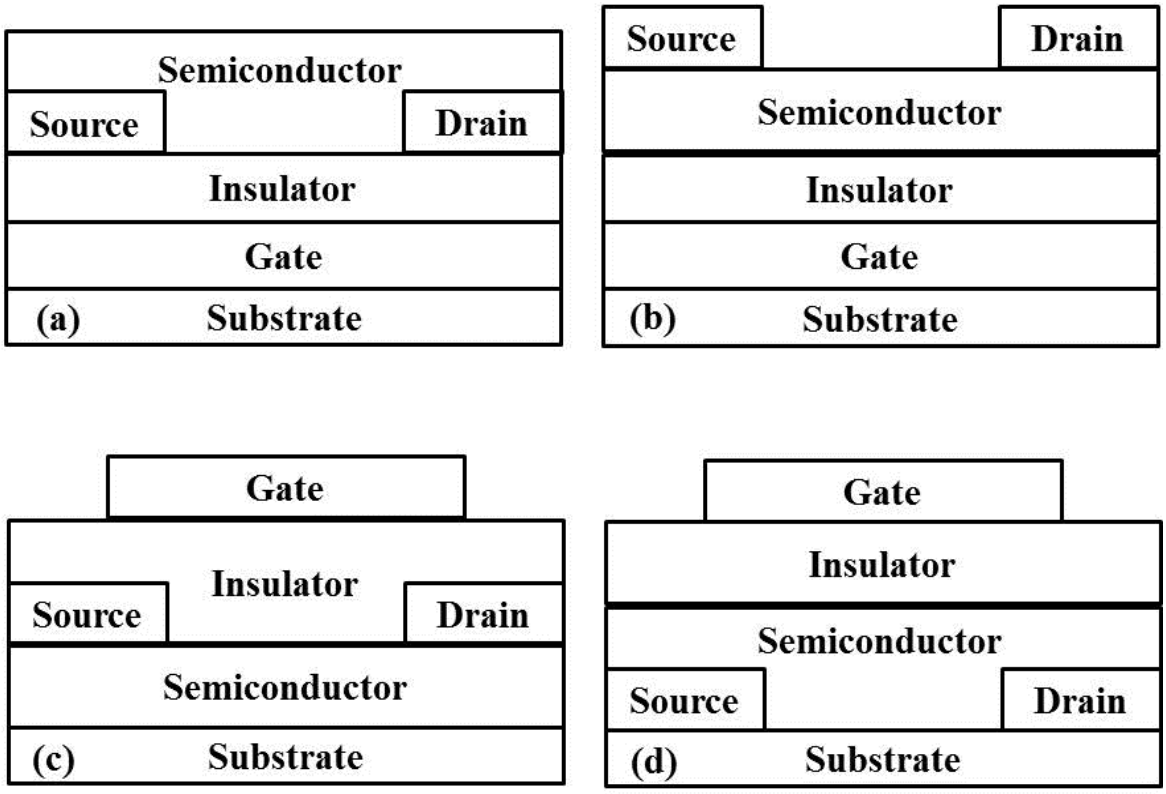

Fig.2.1.1 Cross-sections of simplified OTFT device configurations: (a) Inverted-coplanar structure (bottom-contact); (b) Inverted-staggered structure (top-contact); (c) Top-gate coplanar structure; (d) Top-gate staggered structure.

2.2 Device Operation

The basic device operation can be explained using a bottom-contact OTFTs as an example, as shown in Fig.2.2.1 (a). An OTFTs device can be considered as two capacitor plates separated by an insulator. One capacitor plate can be perceived as a conducting channel sandwiched between source and drain contacts, with the second plate of the capacitor located at the gate contact. The charge carrier density on this plate is modulated by the voltages applied to the three terminals: the source, the drain, and the gate.

The gate and the drain are both negatively biased and the source is grounded for a p-channel OTFT within a p-type organic semiconductor, as shown in Fig.2.2.1 Positive charges (holes) are injected from the source into the active layer (semiconductor), and then are accumulated at the semiconductor/insulator interface by the strong electric field across the insulator. The charges with opposite sign (electrons) are induced along the insulator/gate interface as in an ordinary capacitor. The newly formed charge carriers (accumulated holes at the semiconductor/insulator interface) generate a conducting channel between the source and the drain if their mobility is high enough and the charge carriers are not trapped. The accumulated charge carriers move (drift, hop, or tunnel) under the influence of the drain-source field and enter the drain. If the insulator has a capacitance per unit area, C_{OX}, then the accumulated charge density is simply $C_{OX}\ V_G$, assuming that the voltage drop across the semiconductor and the insulator is negligibly small. For a large negative gate bias and low drain bias, the accumulated charge carrier density is uniform throughout the conducting channel as seen in Fig.2.2.1 (a). Assuming a constant

mobility, the channel current increases linearly with the accumulated charge density $C_{OX}\ V_G$ induced in the channel due to a voltage increase at the gate contact [3].

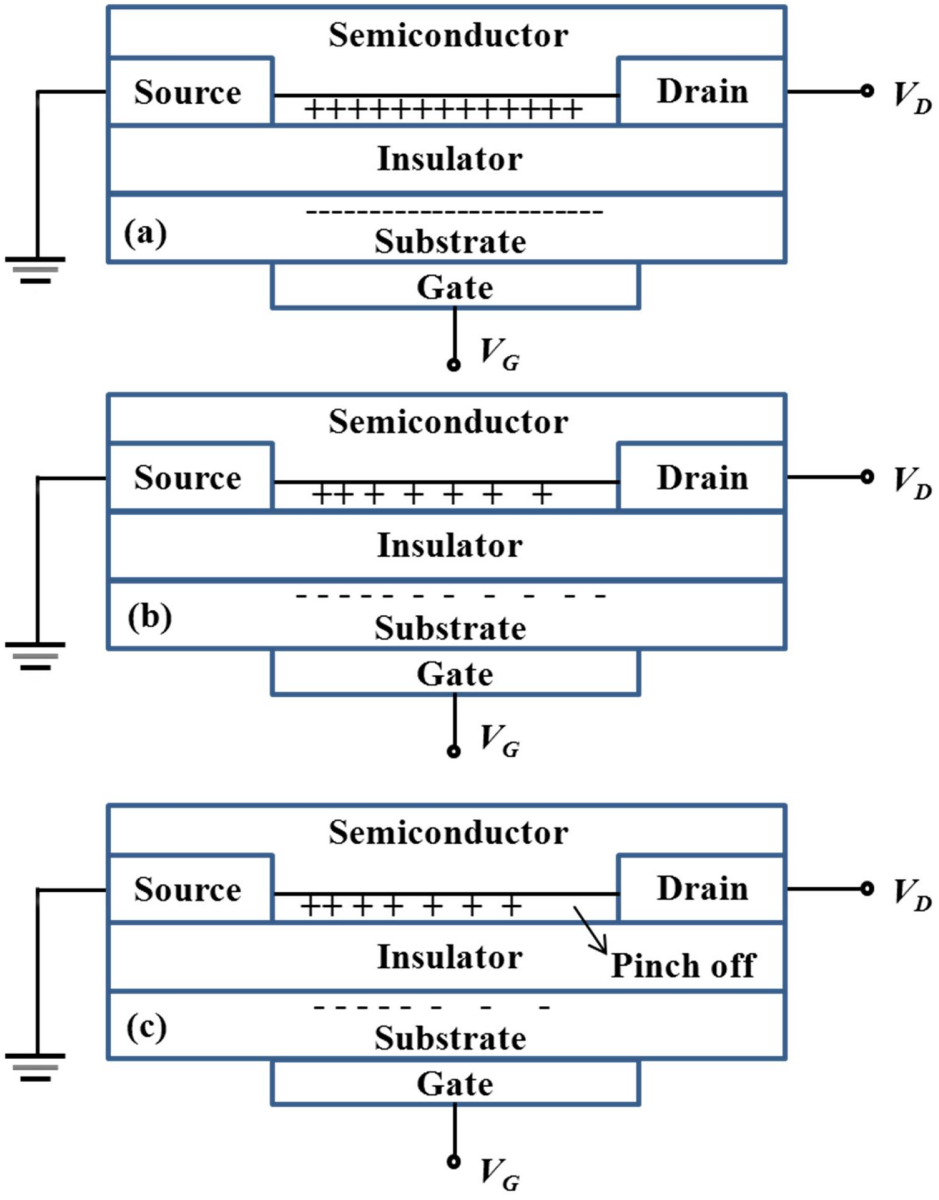

Fig.2.2.1 Schematic diagram of OTFT operation. ñ+ò represents a positive charge (hole) in the conduction channel and ñ-ò represents its opposite charge (electron).The schematic diagram describes the development of the positive accumulation region (a), non-uniform charge density in the channel (b), and the depletion region by the drain contacts (c), respectively. The arrow shows the injection direction of holes.

This is also characterized as a linear regime. As the drain bias becomes increasingly negative, the voltage drop over the insulator and semiconductor becomes a function of the position in the channel as shown in Fig.2.2.1 (b). At the source contact, the voltage drop and accumulated charge density will remain the same. At the drain contact the voltage drop decreases, giving rise to a lower accumulated charge density, and the accumulation charge density will decrease from the source to drain contact. If the drain becomes more negative than the gate then a depletion zone begins to appear and grow from the drain contact as shown in Fig.2.2.1 (c). The channel at the drain side is pinched off and the current increases sub linearly and even saturates. This is characterized as a saturation regime.

2.3 Electrical Characterization of OTFTs

2.3.1 Current-Voltage (*IV*) Characteristics

Several analytic models have been developed to describe current-voltage characteristic in OTFTs [3-7]. These models, based on the well-developed MOSFET model, usually incorporate the contact effect, field-effect mobility and other effects to account for non-linear effects in OTFT characteristics. However, the parameters calculated and reported in the OTFT literature are mostly extracted using expressions of drain current derived from traditional inorganic MOSFET model.

Using pentacene as an example, p-channel OTFT operation can be described using a square-law model developed for MOSFET. The regions are usually determined by the values of applied voltages V_G and V_D in the MOSFET. As shown in Fig.2.3.1 the device is operated in the linear

regime for $|V_D| \leq |V_G\text{-}V_T|$ and is operated in the saturation regime for $|V_D| \geq |V_G\text{-}V_T|$. Here, V_T is the threshold voltage.

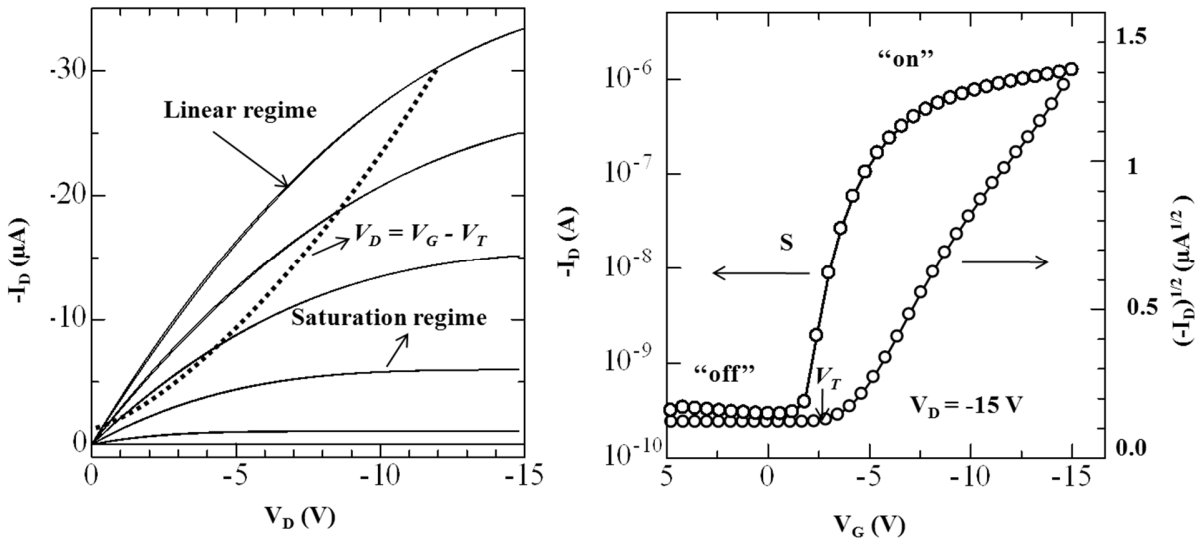

Fig.2.3.1 Typical electrical characteristic of pentacene based OTFTs: (a) I_D-V_D output curve and (b) transfer characteristic.

In the linear regime for $|V_D| \leq |V_G\text{-}V_T|$, the drain voltage V_D is very low and the current varies linearly with it. The channel regime functions as a resistor and can be described as below:

$$I_D = -\frac{W}{L}\mu C_{OX}[(V_G - V_T)V_D . - \frac{{V_D}^2}{2} \qquad (2.3.1.1)$$

For small V_{DS} ($|V_D| << |V_G\text{-}V_T|$), the second term in the square bracket can the ignored and Equation (2.3.1.1) can be simplified as:

$$I_D = -\frac{W}{L}\mu C_{OX}[(V_G - V_T)V_D . \qquad (2.3.1.2)$$

Where W and L are the channel width and channel length, C_{OX} is the capacitance of the insulator, μ is field-effect carrier mobility, V_G, V_D and V_T are the gate, drain and threshold

voltages respectively. W (width) and L (length) are the dimensions of the semiconductor channel defined by the source and drain electrodes.

As drain voltage increases until $|V_D|$ is larger than $|V_G\text{-}V_T|$, is larger than, the drain current becomes independent of the drain voltage and varies as the square of the gate-source voltage as shown in Equation (2.3.1.3). In this case, the device operates in a saturation regime.

$$I_D = -\frac{W}{2L}\mu\, C_{OX}\left(V_G - V_T\right)^2. \qquad (2.3.1.3)$$

This model is based on the gradual channel approximation and assumes that the field-effect mobility is independent of the gate voltage, and that the source/drain contacts are Ohmic [8, 9]. Therefore, the expression above does not account for the non-linear behavior of drain current at low drain bias generally observed in inorganic TFTs and OTFTs.

2.4 Extraction of Electrical Parameters

2.4.1 Mobility

Field effect mobility is the average charge carrier drift velocity per unit electric field and measure of how easily charge carriers can move in the device. Large mobility is required for reliable operation of transistor. Due to weak intermolecular interaction in the solid material state, impurities, defects and inefficient carrier injection capability at the metal contacts, OTFTs are characterized with much lower carrier mobility than inorganic MOSFETs. In 2010 Hagen proposed a solution by self-assembled monolayer in combination with a high quality insulating

layer called multilayer [10]. Mobility increases with increase in channel length and active semiconductor layer thickness. The mobility of organic thin film transistor is gate biased dependents and tends to increase when gate bias increases.

The carrier field-effect mobility in the linear regime can be extracted from the transconductance g_m which is the change of I_D with V_G for a small drain voltage V_D.

From Equation (2.3.1.2), it is given by

$$g_m = -\frac{\partial I_D}{\partial V_G}\bigg|_{V_D-small\ const.} = -\frac{W}{L}\mu\, C_{OX} V_D. \qquad (2.4.1.1)$$

Therefore, the linear mobility μ solved from Equation (4) is given as:

$$\mu = -g_m \frac{L}{W}\frac{1}{C_{OX}}\frac{1}{V_D}\bigg|_{V_D-small\ const.}. \qquad (2.4.1.2)$$

The field-effect mobility in the saturation regime is also extracted from the transfer characteristics (I_D *vs.* V_G) for the device biased as $|V_D| \geq |V_G\text{-}V_T|$. Equation (2.3.1.3) shows that the square root of the saturation current is linearly dependent on the gate voltage. The field-effect mobility can be extracted from the slope of the curve which plots the square root of the saturation current as a function of gate voltage V_G, as shown in Fig.2.3.1 (a). The mobility can be calculated from Equation (2.3) and is given as:

$$\mu = 2\frac{L}{W}\frac{1}{C_{OX}}\left(\frac{\partial\sqrt{I_D}}{\partial V_G}\right)^2 \qquad (2.4.1.3)$$

2.4.2 I_{on}/I_{off}, Threshold Voltage (V_T) and Sub threshold Voltage (S)

The ratio of current in the accumulation mode over the current in the depletion mode is called I_{on}/I_{off}. Current ratio depends upon various factors such as materials, channel length, and thickness of semiconductor. Short channel devices exhibit higher on/off current ratio over larger channel length. To extract information about impurity concentrations, interface states and traps it is common practice to use threshold voltage and sub threshold current as device evaluation parameters. The threshold voltage V_T of OTFTs varies with either the gate insulator capacitance or the thickness of the organic film. The devices with shorter channel length and thicker Pentacene films tend to have smaller threshold voltages. Lower V_T is useful in lowering device power consumption and useful in producing portable devices.

Transfer characteristics (V_G *vs.* I_D) are often plotted on a logarithmic scale, as shown in Fig.2.3.1 (b),which gives access to other important parameters, such as on-off current ratio I_{on}/I_{off}, Threshold Voltage V_T and sub threshold slope *S*. Note that the negative I_D current is normalized in order to characterize it on a logarithmic scale. I_{on}/I_{off} is the ratio of the maximum I_D (ñonò current) value to the minimum I_D (ñoffò current) value, obtained from transfer characteristics plotted on a logarithmic scale as shown in Fig.2.3.1 (b).

Sub threshold slope S is defined as the rate at which I_D varies (in decades) with V_G for device operation in the sub threshold region. It describes the turn-on characteristics of the device and is given as:

$$S = \frac{\partial V_G}{\partial(\log I_D)} \qquad (2.4.2.1)$$

S can be extracted by fitting a line to the steepest part in the sub threshold region and calculating its inverse.

2.4.3 Contact Resistance

Generally, contact resistance originates from disturbed crystal growth at the edge of metal contacts and a contact barrier at the interface of the metal/organic semiconductor. The film at the edge of the contact is quite rough, and pentacene cannot form a well-defined terrace. Smaller crystal size at the edge forms a large number of grain boundaries that contain many morphological defects (e.g. void spaces). Those defects play a role as charge-carrier traps which is considered to be responsible for the degraded performance in bottom-contact pentacene OTFTs [4].Large contact barrier usually exists when injection or extraction of electrons occurs from the metal contact to organic semiconductor. Unlike in conventional MOSFETs, the metal contacts in OTFTs cannot be modified by traditional doping methods, such as ion implantation, diffusion, etc. The barrier height depends on the HOMO and LUMO levels of the organic semiconductor relative to the work function of the metal. The voltage drop across the contact area cannot be negligible compared to the drop across the active region of the channel. For OTFTs, the contacts are generally not Ohmic, and the resistance associated with carrier injection and extraction is not the same. This has been confirmed using scanning potential imaging [10] and scanning Kelvin probe measurement [11]. Z. Bao et. al. give a clear introduction to what an ohmic contact is and what the origins and techniques used to quantify the contact resistance are can be found in Ref. [12]. Ideally the contact resistance should be Ohmic and small in order to make enable the whole voltage applied to the device, contributes to the transport current. For top

contact devices it strongly depends upon gate bias and sharply increases at low gate-source voltage, while contact resistance appears to be almost independent of the gate bias in bottom contact structures. Nowadays, it is an accepted idea that its value decreases with increasing gate voltage, and for this reason the mobility estimated in the linear regime may be substantially smaller than that extracted from the saturation region. Interesting theoretical works have been carried out to explore this effect in a staggered device and important considerations on the dependence of the resistance on the applied voltage have been provided [13, 14]. In top contact structure the field effect mobility is higher and contact resistance is lower due to large injection area whereas contact resistance is higher in bottom contact devices due to poor morphology.

2.4.4 Effect of Channel Length

Drain current strongly depends upon the semiconductor used for channel and it can be modulated by length of the conducting channel. M. Austin et al quoted drain current dependence on the length of channel for P3HT (poly (3- hexylthiophene)) in OTFTs with different channel lengths of 1000nm and 70nm. It has been shown that saturation region was present for long channel (1000nm) device but no saturation region appeared in the short channel (70nm) device. Long channel devices are relatively immune to high contact resistance and when scaled to smaller channel lengths, the device performance may degrade [15]. In a recent feature article, the group of von Seggern demonstrated how the type of the channel can be change from p to n by controlling the localized trap states at the dielectric surface, in both SiO_2 and polymeric insulators [16].

Although much progress has been made developing semicon-ducting polymer devices with higher mobilities, device performance can be improved by reducing the channel length [17]. Previous attempts at fabricating short-channel devices included electron-beam lithography (EBL), phase shift masks, and cold welding metal transfer [18-21].However, in order to realize the low-cost advantage of using polymers, the lithography process must be capable of high-throughput, inexpensive, submicron patterning, qualities that previous techniques have yet to fully demonstrate [22].

2.4.5 Effect of Active Layer Thickness

Electrical parameters of OTFT does not solely depend upon gate capacitance, these can be modulated by film thickness and charge injection from the source electrode. There are trends which can be expressed as a function of the product of thickness of polymeric film and gate capacitance per unit area. It has been observed that with increasing the permittivity of gate insulator and thickness of organic material, the mobility decreases in OTFTs [23].

2.5 Limitations

Almost all electronic devices used in daily life are based on inorganic semiconductors, silicon or gallium arsenide, since they are extremely stable. It's essentially impossible to destroy silicon. Organic semiconductors are very soft and sophisticated. They degrade and can break easily. Characteristics of organic materials changes with environmental conditions after long duration. So the stability of these devices has to be worked out and modeled properly to better understand the process of degradation. Researchers agree that most of the instability comes from the

chemical structure of the compound, and they are trying to find ways to make more stable organic compounds. Furthermore, the OTFT current-voltage characteristics degrade at higher temperatures and the noise at low frequency increases. Scientists throughout globe are intending to develop organic semiconductor with high mobility and fast switching time.

2.6 Device fabrication and Material Used

The transistor devices were fabricated in a cleanroom. All process steps were carried out in ambient atmosphere and at room temperature unless otherwise noted. All the transistors reported in the included papers have a bottom-gate top-contact configuration, Device fabrication include substrate, gate electrode, gate insulator semiconductors and source/drain electrodes. The general manufacturing process and materials used for the fabrication of such pentacene-based top-contact OTFTs is presented below.

2.6.1 Substrate

The low temperature fabrication process for OTFT allowing great freedom for the choice of substrate materials. Plastic substrates, in particular, allow circuits to be fabricated directly onto smart cards and inventory tags, and open up the possibility of rapid, high volume web processing. Rugged, flexible displays can also be built using an OTFT active-matrix on plastic, with liquid crystal or organic light-emitting diodes (OLEDs) as the electro-optic element. Most organic electronic devices reported so far are fabricated on inorganic substrates, such as glass sheets and silicon wafers, which has limited the intrinsic flexibility of organic semiconductors [24-27.]. When a rigid substrate was replaced by a plastic foil, for instance, polyethylene terephthalate,

polyimide, or polyethylene naphthalate, [28ï 31] the flexibility of organic electronic devices has been partly released. Inorganic substrates have high melting point and good flatness whereas polymer substrates have high toughness, flexibility and light weight. In present study the devices were fabricated by using Corning 1737 AMLCD (2.5× 2.5 mm) glass substrates. Glass has a very low transmission of liquid water and water vapor while still being transparent, which prevents damage to the device chemically in addition to physical protection. Glass also is a good insulator so electrical devices placed upon it will not leak current by conduction. Prior to use the glass substrate were ultrasonically cleaned by using organic solvents, like acetone, semi co clean and deionizer water. After that the substrate were dried by air gun before further processing is performed.

2.6.2 Gate Electrode

For the fabrication of top contact OTFT after the substrate preparation, the next step will be the deposition of gate electrode. As OTFTs scaled in physical dimension around the 100 nm technology scale, the integration of high permittivity dielectrics and metal gate electrodes into organic devices gate stacks will be required. Metal gate technology is particularly attractive because it eliminates the poly-Si gate depletion effect and the associated degradation in transistor performance [32-34]. In thermally grown SiO_2 substrate the gate oxide leakage is increasing with decreasing SiO_2 thickness and SiO_2 is running out of atoms for further scaling. The high- k/metal gate combination is also important for enabling future high-performance and low gate leakage in OTFTs [35-37]. Metals are also generally more compatible with alternative gate dielectric or high-permittivity (high-k) gate dielectric materials than poly-Si. The urgent need for alternative

gate dielectrics to suppress excessive transistor gate leakage and power consumption could speed up the introduction of metal gates in complementary metal oxide semiconductor (CMOS) transistors. To achieve high performance and low gate-leakage current Tantalum (Ta) metal gate electrode was used in this study. The (Ta) gate electrode was deposited by using RF sputtering.

2.6.3 Gate Dielectric

In the early times of organic electronics, the attention was essentially focused on the active layer. The large majority of the devices were made on silicon oxide thermally grown on single-crystal silicon wafers. Nowadays, it is widely recognized that the physical properties of the organic semiconductor are not the only parameters to be taken into account for the final performance of OTFTs. So even if the well-known properties and well-mastered technology of silicon microelectronics still provides a sound basis for the search of organic semiconductors with high mobility and stability, great interest is given to other insulating materials, for example, polymeric dielectrics, that offer the possibility of obtaining large area devices through simple and inexpensive solution processes. A critical issue that limits the performance of organic transistors is the large operating voltage that arises from poor capacitive coupling as a result of the thickness and the low dielectric constant of the insulating layer. This is especially true in the case of organic insulators which in many cases are preferred to the higher dielectric materials because of the lower mobility registered in the latter case. An interesting way to get around this problem is to use low-thickness insulating layers with high dielectric constants. The insulator also plays a leading role in the characteristics of the device and the motion of carriers is critically determined by the intrinsic properties of the semiconductorï insulator couple, by directly affecting the

semiconductor structural order. It has an effect on the flow of carriers in both polymeric and more ordered small-molecule-based semiconductors. Generally speaking, a high-performance transistor comprises a surface-smooth dielectric layer in which charge injection from the gate does not occur and which is free of static charges, for example, as a result of interfaced trapped carriers that might disturb the threshold voltage of the device. The dielectric material needs to have very high resistivity to prevent the leakage between gate and semiconductor channel and highest possible dielectric constant to have enough capacitance for channel current flow. Polymers have good processability and dielectric properties. Low switching voltage of OTFTs was obtained by high dielectric constant insulators. For this, we are oriented to other insulators which have a high dielectric constant called as high-k. Among the most used high-k materials Tantalum oxide (Ta_2O_5), Hafnium dioxide (HfO_2), titanium dioxide (TiO_2) and Polymethylmethacrylate (PMMA) were highly used. Tantalum oxide (Ta_2O_5) is a potential material alternate to the conventional insulators like silicon dioxide and silicon nitride for applications as capacitors in dynamic random access memory devices. Ta_2O_5 shows high-k and it seems to be the most promising candidate as insulators for high performance OTFTs because of its high dielectric constant, thermal stability and adequate breakdown voltage. Lower functioning voltage has been observed with Ta_2O_5 insulator layer. The deposition of Ta_2O_5 has been widely studied by many techniques such as thermal oxidation [38, 39], anodic oxidation of tantalum [40], reactive sputtering [41], chemical vapor deposition (CVD) [42], plasma-enhanced chemical vapor deposition (PE-CVD) [43] and RF magnetron sputtered [44]. In the present investigation, Ta_2O_5 is used as insulator and deposited by RF magnetron sputtering by using oxygen and argon partial pressures.

2.6.4 Source Drain Electrodes

For electrode metals such as gold (Au), platinum, aluminum, magnesium, copper and chromium was highly used. Among the entire metal electrodes, Au electrodes were highly used in organic devices. The high work function of Au metal leads to considered an essential element for a good matching between the energy levels at the metalï semiconductor interface. However, this is not the only possible choice. Lower contact resistances are also obtained using copper in a pentacene TFT instead of gold, in spite of the fact that the former has a lower work function than the latter, so that a worse level alignment is expected. In present research Au were deposited by using thermal evaporation. However for the Gate electrode the tantalum Ta metal is deposited by using RF sputtering.

2.6.5 Organic Semiconductors

Research on organic semiconductors started in the 1970s and since then several devices such as LEDs and TFTs have been fabricated using organic materials [45]. The advantages of organic materials over the inorganic ones are the ease of processing due to their unique mechanical properties. They can be vacuum deposited at low temperatures, drop cast or spin coated from solution. The main difference between organic and inorganic semiconductors is that charge transport takes place in well-defined bands in the case of inorganic crystalline semiconductors, and as a stochastic process of hopping between localized states in organic materials. This gives rise to the low carrier mobility in organic semiconductors compared to their single crystal inorganic counterparts. Organic semiconductors can be arranged in three different groupôs fully conjugated polymers, heterocyclic oligomers and polyaromatic rings. Thiophene oligomers are

among the best small organic molecules in terms of mobility. Pentacene has shown the highest mobility among the p-type organic materials and is one of the most promising materials for the OTFTs [46]. A mobility as high as 35 $cm^2\ V^{-1}s^{-1}$ has been obtained in a single crystal pentacene deposited by vacuum sublimation [47], which is two orders of magnitude higher than is observed in rr-P3HT [48]. Use of an evaporation method produces a pentacene film with a mobility of about 1 $cm^2\ V^{-1}s^{-1}$, which is the same as the mobility in amorphous silicon [49].

Pentacene is a polyaromatic hydrocarbon that consists of five linearly fused aromatic rings. It is a flat molecule and the carbons can be numbered in the way. Pentacene is a conjugated molecule and as already mentioned it is the most promising organic semiconductor because of its excellent transistor characteristics. The chemical structure of pentacene is shown in Fig.2.6.5.1. The conjugated structure produces a delocalized carrier over the entire molecule. However, the conjugation length is limited to a very short range by the size of the molecule. When grown by evaporation in high vacuum, pentacene forms a film with a favorable crystal geometry and orientation. Due to the morphology of the films, there is a good intermolecular overlap that leads to the high mobility that is measured. The molecules are arranging themselves into a so-called herringbone structure with their molecular axes perpendicular to the substrate. When the lattice-structure is observed, two types of intermolecular interactions can be distinguished. There is an interaction between the S-orbitals of molecules that lay parallel to each other and this interaction is called as face to face interaction. Between the molecules that are not oriented in a parallel way to each other, there is an œedge to faceô interaction. Here the S-system of one molecule is interacting with the hydrogens of the other molecule. These interactions are responsible for the high mobility and on/off ratio. In spite of these high quality properties, the practical use of

pentacene in organic thin-film transistors (OTFTôs) has some drawbacks caused by its sensitivity to oxygen and low solubility, as mentioned at the beginning of this work. Due to the extremely low solubility of pentacene, only deposition by evaporation is possible. Until very recently, this was only possible with ultra-high vacuum equipment. Because of the cost and the difficulties of the production of large-area electronics, this is a severe disadvantage for industrial purposes. A second problem caused by the lack of solubility, is the difficulty chemists experience while trying to purify pentacene with common techniques. The commercially available pentacene is not pure enough for use in OTFTôs. This necessitates intensive purification by train sublimation.

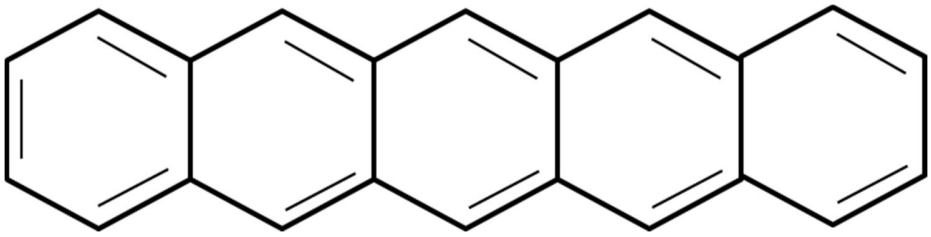

Fig.2.6.5.1 Structure of Pentacene

2.6.5.1 Deposition Methods for Organic Semiconductors

Polymers can be deposited from solution by spin-coating or printing, the small molecule in turn is deposited from thermal evaporation under vacuum, because almost all the small molecules used in OTFT are insoluble. The organic material used in this thesis is the p type semiconductor pentacene. Several methods exist for the deposition of such organic semiconductors. Vacuum evaporation and deposition from solution either by drop casting or spin coating of soluble organic semiconductors are the mostly used depositions techniques [50-53]. The physical properties of the resulting organic semiconductor layer such as morphology and charge transport

are strongly influenced by the details of the deposition procedure. Additionally, the substrate properties are very important to determine the morphology of the deposited. The main reasons why organic semiconductors are attractive for applications is the relatively simple and/or inexpensive deposition methods required for these materials in contrast to their inorganic counterparts.

2.6.5.2 Thermal Evaporation

Several methods exist for the deposition of organic semiconductors. The physical properties of the resulting organic semiconductor layer such as morphology and charge transport are strongly inþuenced by the details of the deposition procedure. Organic electronic devices based on short molecules such as acenes and thiophenes are usually fabricated by thermal evaporation in vacuum because of the insolubility of these materials. An electrically heated boat containing the pentacene material is placed inside a vacuum chamber at certain distance from the boat the substrate was placed. A careful control of the evaporation conditions including substrate temperatures as well as the evaporation rate allows depositing highly ordered pentacene films. For instance, the grain size of pentacene has been found to depend critically on the substrate temperature, vacuum pressure and deposition rate. Evaporation temperatures for organic semiconductors are lower than the required for inorganic semiconductors. The only drawback is that it is a time consuming process because of the time required to pump the evaporation chamber. Due to the high degree order that can be achieved with the evaporation process the mobilities associated with device using this method are in general higher than with solution processes.

2.7 Other Fabrication Techniques

2.7.1 Photo Resists Coating

For patterning of the device the substrate is loaded on a spinner to coat it with photoresist. First, the substrate was coated with a layer of hexamethyldisilazane (HMDS) as an adhesion layer and after that a layer OFPR-800 photoresist was coated. 1 or 2 ml of HMDS and OFPR-800 was dropped on the surface of the wafer by means of a glass pipette so as to cover the surface. Both the coating were spun for 5 sec at a speed of 500 rpm and 60 sec at a speed of 3000 rpm.

2.7.2 Soft Baking

It is recommended to wait about a minute before removing the substrate from spinner in order to dry the film. The photoresist is then baked to make a film that is stable for light exposure. The process is called soft baking, in which the photoresist was heated while placing the substrate on hotplate for 60 sec at 80 °C.

2.7.3 Mask Alignment and Exposure Conditions

A photo mask was to apply the desired pattern. The photoresist coated wafer is loaded and following that the mask is put in the mask aligner. The contact mode is chosen which puts the mask on top of the sample without any gap between the two. Then UV light is shined for 8 s. The exposure timing for the UV light is very critical as under exposing or overexposing causeôs non developed or over developed patterns. Therefore its very important that the user will check the calibration of the light intensity regularly.

2.7.4 Developing

The non-exposed area of the photoresist is chemically more resistant, whereas the exposed area was washed away more readily by the developer. The NMDW developer solution was used. Around 100 ml of NMDW was placed beaker and then the substrate was kept in the beaker. In ~2 minutes the pattern appears on the photoresist while the user is shaking the bath. The sample is then put in a water bath (deionized) for about 2 minutes to wash the developer from the sample. It is then dried using air gun. For micron scale feature sizes it is recommended to check the pattern using an optical microscope to be sure that the pattern is well developed. If it is underdeveloped, it can be put back into the developer solution for one minute more, but if it is overdeveloped, the photoresist has to be removed from the surface and the process started over again. For the etching process the substrate were backed again for 60 sec at 80 °C. Chemical and Reactive ion etching was used in this study.

2.7.5 Lift off

To remove the photoresist the sample is sonicated in acetone for about 5 minutes. The buried photoresist lifts off and the metallic micro-electrodes stay on the surface of the substrate. Then the sample is washed with acetone to remove the chemical residue and rinsed with deionized water and dried with air gun.

2.8 Device Characterization

In this section we will review the main electrical and microscopic characterization techniques used for investigation of organic electronic devices.

2.8.1 Electrical Characterization

Electrical characterization techniques are the aggregate of techniques applied in OTFTs for the characterization of charge carrier traps and carrier transport properties in organic semiconductor materials. The material is usually processed into a very thin film through which a current passes. Thus, the ability to characterize transport properties of an organic film is of special importance in organic electronics. In these experiments, the mobility measurement can be performed if the organic active layers are amorphous. In the OTFT experiment, the organic active layers are commonly thin and ordered, and other electrical characterization techniques are also well applied for the carrier measurement. The experimental set-up used for current-voltage characterization of the fabricated organic electronic devices. Later, results of the results of these measurements are given. Electrical measurements were performed at room temperature using a semiconductor parameter analyzer (HP 4155B). The drain current Vs drain voltage (I_D-V_D) curves with varying temperature at a fixed gate voltage of 0 V are measured for investigation of carrier transport properties by loading the fabricated devices into a cryostat. The temperature was varied from 133 to 293 K by flowing liquid nitrogen into the sample holder in the vacuum chamber.

2.8.2 Microscopic Characterization

All the challenges relating to organic transistors are actually on the micro or nanoscale level. In order to meet these challenges, there is a clear need for characterization techniques to correlate our macroscopic manipulation with important properties of organic electronic devices. Therefore, in this section we will introduce the tools available for the characterization of OTFTs. The

surface morphology including root mean square roughness of pentacene layer was characterized by using atomic force microscopy techniques.

2.8.2.1 Atomic Force Microscopy

AFM belongs to the family of scanning probe microscopy (SPM) techniques where a sharp probe is scanned across the sample surface and some probe-sample interaction is monitored. The resulting AFM image is directly related to the surface topography because it is based on scanning the atomic force between a sharp tip attached to a cantilever and the atoms on the sample surface. Another form of SPM is scanning tunneling microscopy (STM). AFM uses a sharp tip attached to the end of a cantilever and can operate in three operation modes. In contact mode AFM the change in cantilever deflection is monitored by the system and the feedback loop maintains a constant cantilever deflection. The vertical displacement to keep the cantilever deflection is recorded to produce the topographic image. This is the only AFM technique capable of atomic resolution. In tapping mode AFM the cantilever oscillates at a frequency around resonance with amplitude in the range between 20 and 100 nm. The tip contacts the sample surface at the bottom end of the oscillation. The feedback maintains constant the amplitude of the oscillation and the vertical position is recorded. Finally, in non-contact mode AFM the cantilever oscillates at a frequency slightly above the resonance frequency with amplitude shorter than 10 nm. The tip oscillates above the adsorbed fluid layer on the surface. The feedback loop maintains constant the amplitude or the frequency of the oscillation by moving the tip vertically. The resonance frequency of the cantilever is decreased due to the van der Waals and other long-range forces that act 1 to 10 nm above the adsorbed fluid layer.

2.9 References.

[1] G. H. Gelinck, T. C. T. Geuns and D. M. de Leeuw: Appl. Phys. Lett. **77**, 1487, 2000.

[2] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu and E. P. Woo: Science **290**, 2123, 2000.

[3] A. R. Brown, C. P. Jarrett, D. M. deLeeuw and M. Matters: Syn. Met. **88**, 37, 1997.

[4] C. D. Dimitrakopoulos and P. R. L. Malenfant: Adv. Mat. **14**, 99, 2002.

[5] G. Horowitz: Adv. Mat. **10**, 365, 1998.

[6] G. Horowitz: Semicon. Poly. 463, 2000.

[7] E. Calvetti, L. Colalongo and Z. M. K. Vajna:: Solid-State Elec. **49**, 567, 2005.

[8] M. S. Shur, Physics of Semiconductor Devices. New Jersey: Prentice-Hall, 1990.

[9] R. F. Pierret, Semiconductor Device Fundamentals: Addison-Wesley, 1995.

[10] K. Seshadri and C. D. Frisbie: Appl. Phys. Lett. **78**, 993, 2001.

[11] T. W. Kelley and C. D. Frisbie J. Vac. Sci. & Tech. B: **18**, 632-635, 2000.

[12] Z. Bao and J. Locklin, Eds., Organic Field-effect Transistors, CRC Press, Boca Raton 2007.

[13] N. Tessler and Y. Roichman, Appl. Phys. Lett. **79**, 2987. 2001.

[14] T. J. Richards and H. Sirringhaus, J. Appl. Phys. **102**, 094 510, 2007.

[15] M. Austin and S. Chou: Appl. Phys. Lett. **8**, 4431, 2002.

[16] N. Benson, C. Melzer, R. Schmechel and H. V. Seggern, Phys. Status Solidi A. **205**, 475, 2008.

[17] H. Sirringhaus, N. Tessler and R. H. Friend,: Sci. **280**, 1741, 1998 .

[18] F. Garnier, R. Hajlaoui and M. Kassmi: Appl. Phys. Lett. **73**, 1721, 1998.

[19] J. Collet, O. Tharaud, A. Chapoton and D. Vuillaume: Appl. Phys. Lett. **76**, 1941, 2000.

[20] J. A. Rogers, A. Dodabalapur, Z. Bao and H. Katz: Appl. Phys. Lett. **75**, 1010, 1999 .

[21] C. Kim, M. Shtein, and S. Forrest: Appl. Phys. Lett. **80**, 4051, 2002.

[22] S. Y. Chou, P. R. Krauss and P. J. Renstrom: Science **272**, 85, 1996.

[23] O. Marinov and M. Jamal Deen: J. Vac. Sci. Technol. B. **24**, 4, 2006.

[24] A. R. Brown, A. Pomp, C. M. Hart and D. M. de Leeuw: Science **270**, 972, 1995.

[25] A. Dodabalapur, J. Laquindanum, H. E. Katz and Z. Bao: Appl. Phys. Lett. **69**, 4227, 1996.

[26] M. Bonse, D. B. Thomasson, H. Klauk, D. J. Gundlach and T. N. Jackson: IEDM Tech. Dig. **249**, 1998.

[27] H. Klauk, D. J. Gundlach and T. N. Jackson: IEEE Electron Device Lett. **20**, 289, 1999.

[28] Y. Zhao , C. A. Di , X. K. Gao , Y. B. Hu , Y. L. Guo , L. Zhang , Y. Q. Liu , J. Z. Wang , W. P. Hu and D. B. Zhu:, Adv. Mater. **23**, 2448, 2011.

[29] H. Lim , W. J. Cho , C. S. Ha , S. Ando , Y. K. Kim , C. H. Park and K. Lee , Adv. Mater. **14**, 1275, 2002.

[30] U. Zschieschang , F. Ante , T. Yamamoto , K. Takimiya , H. Kuwabara , M. Ikeda , T. Sekitani , T. Someya , K. Kern and H. Klauk , Adv. Mater. **22**, 982, 2010.

[31] J. A. Rogers, Z. Bao, A. Dodabalapur and A. Makhija, IEEE Electronic Device Lett. **21**, 100, 2000.

[32] B. Cheng, M. Cao, R. Rao, A. Inani, P.V. Voorde, W.M. Greene, J.M.C. Stork, Z. Yu, P.M. Zeitzoff and J.C.S. Woo: IEEE Trans. Electronic Devices **46**, 1537, 1999.

[33] I. De, D. Johri, A. Srivastava and C.M. Osburn: Solid-State Electron. **44**, 1077, 2000.

[34] K. Maitra and V. Misra: IEEE Electron Device Lett. **24**, 707, 2003.

[35] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D.

Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White and P. Tobin: Proc. Symp. VLSI Tech. Dig. **9**, 2003.

[36] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros and M. Metz: IEEE Electronic Device Lett. **25**, 408, 2004.

[37] R. Kotlyar, M. D. Giles, P. Matagne, B. Obradovic, L. Shifren, M. Stettler and E. Wang, IEDM Tech. Dig. **39**, 2004.

[38] A. G. Revesz and T. D. Kirkendall: J. Electrochem. Soc. **123**, 1515, 1976.

[39] G. S. Oehrlein and A. Reisman: J. Appl. Phys. **54**, 6502, 1983.

[40] K. Ohta, K. Yamada, R. Shmizu and Y. Tarui: IEEE Trans. Electronic Devices ED. **29**, 368, 1982.

[41] Y. Nishioka, S. Kimura and K. Mukai: in Proceedings of the 165th Electrochemical Society Meeting **160**, 1984.

[42] H. Shinriki and M. Nakata: IEEE Trans. Electron. Devices ED. **38**, 455, 1991.

[43] R. A. B. Devine, L. Vallier, J. L. Autran, P. Paillet and J. L. Leray: Appl. Phys. Lett. **68**, 1775, 1996.

[44] S. V. J. Chandra, G. M. Rao and S. Uthanna: Cryst. Res. Technol. **42**, 290, 2007.

[45] J.M. Shaw and P.F. Seidler: Organic electronics IBM J. RES. & DEV. **45**, 3, 2001.

[46] G. Horowitz: J. Mater. Chem. **9**, 2021, 1999.

[47] O. D. Jurchescu J. Baas and T. T. M. Palstra: App. Phys. Lett. **84**, 3061, 2004.

[48] T. B. Singh and N. S. Sariciftci: Mater. Res. **36**, 199, 2006.

[49] C. R. Kagan and P. Andry: New York: Marcel Dekker, Inc. 2003.

[50] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu, and E. P.

Woo: Science, **290**, 2123, 2000.

[51] D. Zielke, A. C. Hubler, U. Hahn, N. Brandt, M. Bartzsch, U. Fugmann, T. Fischer, J. Veres and S. Ogier: App. Phys. Lett. **87**, 123508, 2005.

[52] F. Xue, Y. Su and K. Varahramyan: IEEE Trans on Electronic Devices **52**, 1982, 2005.

[53] F. Eder, H. Klauk, M. Halik, U. Zschieschang, G. Schmid and C. Dehm: App. Phys. Lett. **84**, 2673, 2004.

Chapter 3

Charge Injection and Organic/Metal Contact in Organic Thin-Film Transistors

3.1 Charge Injection in OTFTs

It is generally recognized that interfaces play important roles in organic semiconductor devices. Taking metal/organic interfaces as an example, the contact between a metal electrode and a single, a small group, or a thin ýlm of molecules can play a critical, if not dominant, role in the performance of molecule-based electronics. The central issue is: how does an electron cross a metalï molecule interface? From a theoretical perspective, a quantitative answer to this question consists of three components: energetic alignment, electronic coupling, and dynamic localization due to polarization in nuclear coordinates. These three concepts are not unique to molecular electronics but have been at the center of chemisorption studies [1].

The schematics of an ideal Schottky barrier formed between a metal and a semiconductor is shown in Fig.3.1.1. The vacuum level at the metal/semiconductor interface is aligned, and as the thermal equilibrium is reached, the Fermi level of the bulk of the semiconductor is aligned with that of the metal. A charged region in the semiconductor forms with a voltage drop of eVB equal to the contact potential difference between the metal and the bulk of the semiconductor. The interface dipole is established in part to satisfy the thermal equilibrium condition between the two materials. It can be facilitated by the surface states of the semiconductor, either intrinsic or induced by the metal contact.

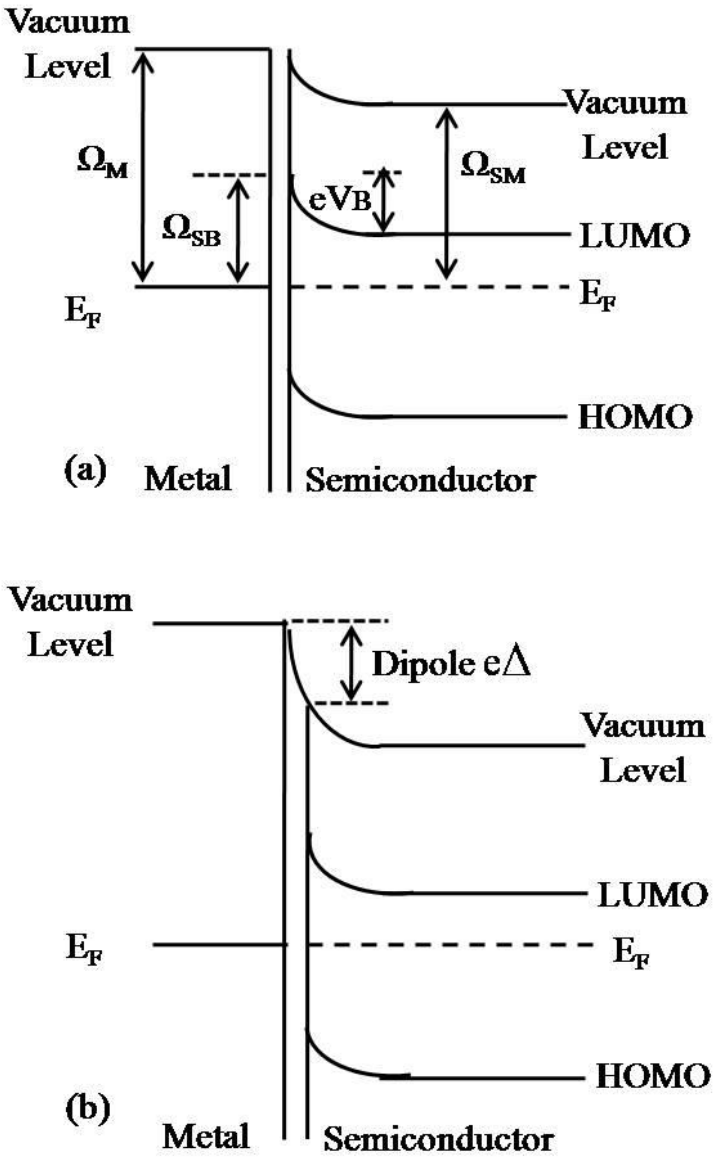

Fig.3.1.1 The schematics of (a) an ideal and (b) a realistic Schottky barrier formed between a metal and a semiconductor. The ideal Schottky barrier height FSB is simply the work function difference between the metal and the semiconductor, FM and FSM, respectively.

For organic semiconductors, the van der Waals nature of the interactions between the molecules results in low energetic expenses in severing the bonds at the surface, and as a result the existence of extensive intrinsic surface states is unlikely. The energy level alignment at the

interface involves a number of physical and chemistry processes. In these processes, the most important ones related to the device performances include possible chemical reaction, interface dipole, diffusion, charge transfer and possible band bending [2-5]. Charge transport in organic semiconductors is a very complex phenomenon. The behavior of organic semiconductors may vary drastically depending on the range of the physical parameters such as temperature, charge carrier density, electric field intensity, energy distribution of carriers, correlation of charge carriers and filling of energy bands. Moreover, it can be further complicated by experimental factors such as presence of charge traps and material inhomogeneity.

3.1.1 Metal Work Function

Despite the considerable progress made in recent years to improve the performance of organic TFTs, many of the design, material, and process parameters are still poorly under stood and poorly controlled. Along with the material properties of each layer in the device, interface properties of the metalï semiconductor [6-10] and insulatorï semiconductor [11-14] have a strong influence on the device performance. Optimization of the interface between the source/drain (S/D) electrode and the organic semiconductor is one of the important factors for the organic thin film transistor (OTFT) performance along with the insulatorï semiconductor interface. In the semiconductorï insulator interface, a channel is formed in the semiconductor side near the interface and carriers flow through this channel. The interface roughness, defects and charges around this region have a strong effect on the carrier life time and the mobility. In the S/D electrodes and semiconductor interface, contact resistance and barrier height will affect the carrier movement through the interface and low barrier height contact is needed [15-19]. With

the decreasing device dimensions, the contact resistance as a part of the total device resistance will dominate over the channel resistance, and therefore the speed of organic integrated circuits may be limited by the contact resistance, not by the intrinsic carrier mobility of the organic semiconductor [20].

3.1.2 Schottky Thermal Injection

If the bottle neck in carrier transport is injection at the contacts, a device is said to be injection or contact limited. In the case of metal/organic layer the interface may show Ohmic or nonlinear I-V characteristics. The band offset between the metal work function and organic layer (depending on whether the transport is p-or n-type) is one important factor in determining the type of contact at the interface. One theoretical approach used to explain the carrier injection results in organic semiconductor devices is the Schottky thermonic emission model [21].

$$I = A^{*}T^{2}\exp\left[\frac{-q\left(\varphi_{B} - \sqrt{qV/4\pi\varepsilon_{i}d}\right)}{kT}\right]. \quad (3.1.2.1)$$

where A^{*} is the effective Richardson constant, T the temperature, φ_B the barrier height at the interface, q the electronic charge, V the applied voltage, ε_i the dielectric permittivity of the mixed organic layer, d the dielectric thickness, and k the Boltzmann constant.

Schottky thermonic emission is usually more significant at high temperatures where the carriers have sufficient thermal energy to overcome the potential barrier. At very low temperatures or in the cases where the height of the potential barrier is relatively large, thermonic emission loses its significance. In such situation, carriers are injected only by means of quantum mechanical

tunneling through the barrier. This process is called field emission and is the dominant injection-limited mechanism at high fields and low temperatures. The *I-V I* predicted by fowler Nordheim equation given below [22].

$$I = \frac{q^3 V^2 m_0}{8\pi h \varphi m^*} \exp\left[-4 \frac{\left(2m^*\right)^{1/2} \varphi^{3/2}}{3hqV} \right], \qquad (3.1.2.2)$$

3.2 Improving Charge Injection

Two different aspects essentially govern the charge-carrier injection: the energy-level alignment at both sides of the interface and the morphology of the active layer in the contact region. Both of these factors are difficult to control, because the presence of an interface dipole most often prevents an easy tuning of the injection barrier height, and the step between the metal and the insulator is always an unavoidable surface energy discontinuity at the origin of disorder in the active layer, particularly in a bottom contact configuration. As a result, a misalignment between the molecules deposited on the metal and on the insulator is difficult to avoid. A recent analysis of pentacene transistors with printed electrodes have, for example, shown devices with relatively high performance comparable with those prepared by conventional lithography processes [23]. This simple technique, compatible with large area micro and nanofabrication, gives devices with a mobility of 0.2 cm^2 $V^{-1}s^{-1}$ and a high on/off ratio of 10^6, but a careful determination of the contact properties have shown that it also leads to higher contact resistance. The charge injection is limited by a poor coverage of the semiconductor at the non-planar edges of the contact. The most important approaches have been employed to reduce contact effects is

certainly the modiýcation the electrode surface by means of SAMs. Using this technique, both an increase of the quality of the semiconductor morphology, [24] and a better matching of the work functions of the two materials [25] can be achieved. It is interesting to note the different effects of the SAMs in the obtained pentacene bottom-contact devices. An improved charge injection has also been reached through other interesting surface treatments [26]. By dipping gold electrodes in a sulfuric acid and hydrogen peroxide mixture prior to pentacene deposition, a high mobility of 0.66 $cm^2 V^{-1}s^{-1}$ was obtained, even with a bottom-contact transistor with a channel length of 3 mm clearly limited by the contacts. In this case, the increase of the performance is attributed to a better energy level matching. Other different approaches employed to reduce contact resistance and to improve charge injection are explained as under.

3.2.1 Doping of Organic Layer

Apart from the bilayer source and drain electrodes, the importance of the active layer doping for an increase of the device performances have been shown recently [27-29]. Working in a top-contact configuration, it is, for example, possible to reduce the resistance of the contact, and consequently increase the on current, by introducing iron chloride as a dopant in the pentacene film. By changing the doping profile under the contact, the effect of the bulk region between the contact and the conductive channel can also be analyzed. The result obtained is that both the resistance connected to the interface, and those related to the bulk of the active layer under the contact can be reduced with the doping process. A lower potential drop in the series resistance leads up to a higher voltage applied to the conductive channel.

As the injecting contacts are usually evaporated or patterned gold electrodes. The high work function of this noble metal leads to it being considered an essential element for a good matching between the energy levels at the metalï semiconductor interface. However, this is not the only possible choice. Some recent works reported, for example, better performance for rubrene single-crystal devices using a nickel source and drain electrodes, although this metal oxidizes in air. Using short-channel contact-limited devices, a lower contact resistance and also a higher reproducibility of the experimental results were achieved even if at the time being there is no clear explanation for these experimental results [30]. Lower contact resistances are also obtained using copper in a pentacene TFT instead of gold [31]. In spite of the fact that the former has a lower work function than the latter, so that a worse level alignment is expected. The interesting explanation for this unexpected better performance is that a narrow exponential trap distribution at the metalï semiconductor interface inþuences the charge motion and a subsequent less resistive region in the semi-conducting ýlm is present near the electrodes.

3.2.2 Bi-layer Electrode System

Other important and commonly practiced approach to overcome the injection barrier for and to reduce contact effects is the modification of the organic/electrode interface by insertion of a suitable charge injection layer. The range of electronic properties of the transition metal oxides offers a unique opportunity to control the work function, and hence, the charge-injection properties. Therefore modification of the organic/electrode interface by inserting a transition metal oxide has received considerable attention in regards to organic electroluminescent devices. Similarly, the source-drain (S-D) contacts in the organic TFTs have significant influence on

device operation, through their contribution to the contact resistance arising from mismatch of the work functions, and/or interaction between the metal electrodes and the organic semiconductor [32-34]. Inserting a metal oxide, such as MoO_3, WO_3, TiO_2, GeO between the S-D contact and organic active layer can greatly reduce the contact resistance for the organic TFTs [35-37]. To achieve the Ohmic characteristics it is necessary that the work function of the metal is closer to the HOMO or LUMO of the organic materials, which lead to enhance the charge injection. For Pentacene/Au contacts there is small mismatch between the work function of Au and HOMO level of pentacene which results to relatively high contact resistance at the Pentacene/Au interfaces. When a metal is directly deposited onto the pentacene, either it will penetrate into the upper layer of pentacene or diffuse into pentacene to form a mixture of metal and pentacene in spite of pure metal. Therefore high contact resistance is observed resulting from the formation of interface dipole barrier which shifts the HOMO level of pentacene downward causing an increase in the difference between the HOMO level of the pentacene and the Fermi level of the Au, hence increasing the barrier height. The highest molecular orbitalôs (HOMO) of pentacene and Au lie at 5.0 eV and 5.1 eV respectively. The HOMO of metal oxide is much deeper than the Au and pentacene and aligned them with the HOMO level of pentacene which reduce the barrier height between the two layers.

3.3 References

[1] X.Y. Zhu: Surf. Sci. Rep. **56**, 1, 2004.

[2] W. Schottky, R. Stormer, F. Waibel: Z. Hochfrequentztechnik **37**, 62, 1931.

[3] S.M. Sze: Physics of Semiconductor Devices,. Wiley, New York, 1981.

[4] C. Kittel and H. Kroemer: Thermal Physics, Freeman, New York, 1980.

[5] B.A. Gregg and M.C. Hanna: J. Appl. Phys. **93** , 3605, 2003.

[6] C. Vanonim, S. Tsujino and T. A. Jung: Appl. Phys. Lett. **90**, 193119, 2007.

[7] J. Park and J. S. Choi: Synth. Met. **155**, 657, 2005.

[8] P. V. Pesavento, K. P. Puntambekar, D. Frisbie, J. C. Mckeen and P. P Ruden: J. Appl. Phys. **99**, 094504, 2006.

[9] P. V. Pesavento, R. J. Chesterýeld, C. R. Newman and C. D. Frisbie: J. Appl. Phys. **96**, 7312, 2004.

[10] K. Ihm, H. E. Heo, S. Chung, J. R. Ahn, J. H. Kim and T. H. Kang: Appl. Phys. Lett. **90**, 242111, 2007.

[11] G. Gu and M. G. Kane: Appl. Phys. Lett. **92**, 053305, 2008.

[12] T. Manaka, E. Lim, R. Tamura and M. Iwamoto: Thin Solid Films **499**, 386, 2006.

[13] T. N. Ng, J. A. Marohn and M. L. Chabinyc: Appl. Phys. **100**, 084505, 2006.

[14] O. D. Jurchescu, M. Popinciuc, B. J. V. Wees and T. T. M. Palstra: Adv. Mater. **19**, 688, 2007.

[15] C. Bock, D. V. Pham, U. Kunze, D. Kafer, G. Witte and A. Terfort: Appl. Phys. Lett. **91**, 052110, 2007.

[16] J. Morgado, A. Charas and N. Barbagallo: Appl. Phys. Lett. **81**, 933, 2002.

[17] Y. Watanabe, H. Iechi and K. Kudo: Jpn. J. Appl. Phys. **46**, 2718, 2007.

[18] S. Y. Kim and J. L. Lee: Met. Mater. Int. **11**, 411, 2005.

[19] J. H. Cho, W. H. Lee, Y. D. Park, W. K. Kim, S. Y. Kim, J. L. Lee and K. Cho: Electrochem. Solid-State Lett. **9**, G147, 2006.

[20] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols and T. N. Jackson: Solid-State Electron. **47**, 297, 2003.

[21] J. Gmeiner, S. Karg, M. Meier, W. Riess, P. Strohriegl and M. Schwoerer: Acta Polym. **44**, 201, 1993.

[22] Z. Chiguvare, J. Parisi and V. Dyakonov: Appl. Phys. Lett. **94**, 2440, 2003.

[23] A. Benor and D. Knipp: Org. Electron. **9**, 209, 2008.

[24] C. Bock, D. V. Pham, U. Kunze, D. Kafer, G. Witte and C. Woll: J. Appl. Phys. **100**, 114517, 2006.

[25] P. Marmont, N. Battaglini, P. Lang, G. Horowitz, J. Hwang, A. Kahn, C. Amato and P. Calas: Org. Electron. **9**, 419, 2008.

[26] T. Maeda, H. Kato and H. Kawakami: Appl. Phys. Lett. **89**, 123 508, 2006.

[27] F. S. K. Fujimori, T. Hamano, T. Minari, T. Miyadera, K. Tsukagoshiam and Y. Aoyagi: Appl. Phys. Lett. **90**, 193 507, 2007.

[28] T. Minari, T. Miyadera, K. Tsukagoshi, Y. Aoyagi and H. Ito: Appl. Phys. Lett. **91**, 053 508, 2007.

[29] C. Vanoni, S. Tsujino and T. A. Jung: Appl. Phys. Lett. **90**, 193 119, . 2007.

[30] A. Molinari, I. Gutierrez, I. N. Hulea, S. Russo and A. F. Morpurgo: Appl. Phys. Lett. **90**, 212103, 2007.

[31] S. D. Wang, T. Minari, T. Miyadera, K. Tsukagoshi and Y. Aoyagi: Appl. Phys. Lett. **91**, 203508, 2007.

[32] Y. Bai, X. Liu, L. Chen, K. Haq, M. A. Khan, W. Q. Zhu, X. Y. Jiang and Z. L. Zhang: Microelectronics Journal **38**, 1185, 2007.

[33] Q. J. Sun, Z. Xu, S. L. Zhao, F. J Zhang, L. Y. Gao and Y. S. Wang: Synthetic Met. **160**, 2239, 2010.

[34] S. D. Wang, T. Minari, T. Miyadera, K. Tsukagoshi, and Y. Aoyagi: Appl. Phys. Lett. **91**, 203508, 2007.

[35] T. Umeda and S. Tokito: Appl. Phys. Lett. **92**, 013301, 2008.

[36] P. Jeon, K. Han, H. Lee, H. S. Kim, K. Jeong, K. Cho, S. W. Cho, Y. Yi: Synthetic Met. **159**, 2502, 2009.

[37] D. W. Zhao, P. Liu, X. W. Sun, S. T. Tan, L. Ke and A. K. K. Kyaw: Appl. Phys. Lett. **95**, 153304, 2009.

Chapter 4

Mobility Enhancement of Top Contact Pentacene Based Organic Thin-Film Transistor with Bi-layer GeO/Au Electrodes

The enhancement of the charge injection and field effect mobility by inserting a thin (5 nm) germanium oxide (GeO) interlayer between the Au electrode and pentacene layer in a top contact pentacene based organic thin-film transistor (OTFTs) was reported. In comparison with the pentacene-based OTFT with only-Au electrode, the device performance has been considerably improved which exhibits the highest field effect mobility of 0.96 cm^2 $V^{-1}s^{-1}$. The improvement was attributed to significant reduction of barrier height at Au/pentacene interfaces and smoothed surface of pentacene layer after inserting a thin GeO layer.

4.1 Introduction

To achieve high performance and high mobility organic thin film transistor (OTFTs), it is very crucial to improve the contacts between the metal electrodes and organic semiconductors. When a metal is directly deposited onto the pentacene, either it will penetrate or diffuse into upper layer of pentacene and form a mixture of metal and pentacene, which causes a large energy difference between the Au Fermi level (EF) and the highest occupied molecular orbital (HOMO) level of pentacene [1-4]. Thus, high contact resistance and hole injection barrier will appear, which limits the device performance and field-effect mobility. Transition metal oxides like molybdenum oxide (MoO_3), tungsten oxide (WO_3), vanadium oxide (V_2O_5) and titanium oxide (TiO_2) and other metal oxides such as aluminum oxide (Al_2O_3) and copper oxide (CuO) have been widely used as bi-layer electrode or hole injection layer (HIL) to reduce the barrier height and contact

resistances at the Au/pentacene interface, which gave better performance and produced higher field-effect mobility compared to the device with only metal electrodes [5-8]. It suggests that the bi-layer electrodes for pentacene based OTFTs could be better scheme for achieving high performance and high field-effect mobility.

In this study, the impact of using GeO and Au as a bi-layer electrode on the electrical characteristics of top contact pentacene based OTFTs was reported. We observed that the performance of the device including field effect mobility, threshold voltage and on/off ratio was highly improved when optimizing the thickness of GeO as 5 nm. Therefore, the combination of 5 nm GeO with Au as bi-layer source-drain electrode could be a promising scheme for achieving high performance in pentacene-based OTFTs.

4.2 Experimental Details

The cross sectional diagram of top contact pentacene based OTFT is shown in Fig.4.2.1. The devices were fabricated by using cleaned glass substrate on which 50 nm thick tantalum (Ta) as gate electrode and 180 nm tantalum oxide (Ta_2O_5) as gate insulator which were deposited by radio-frequency (RF) sputtering. Then, a 40-nm-thick pentacene (Sigma-Aldrich, 98% purity) was thermally evaporated with slow deposition rate of 0.15 Å/s and at a substrate temperature of 60 °C. Finally, the devices were completed by evaporating GeO with varied thickness of 2-20 nm and Au 60 nm onto the pentacene layer through a shadow mask to form bi-layer source-drain electrodes. The devices had a channel length and width of 250 μm and 1 mm, respectively. For comparison, a similar device under same conditions with only-Au electrodes was also fabricated. The electrical measurements were performed at room temperature using a semiconductor

parameter analyzer (HP 4155B). The drain current (I_D) vs drain voltage (V_D) curves with varying temperature were measured for investigation of carrier transport properties by loading the fabricated devices into a cryostat. The temperature is varied from 93 to 293 K by flowing liquid nitrogen into the sample holder in the vacuum chamber. The surface morphology of pentacene films were evaluated using atomic force microscopy (AFM).

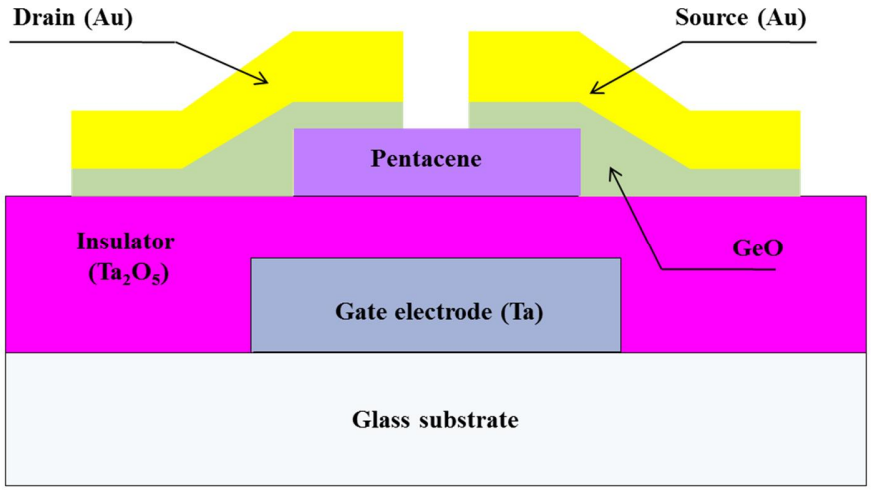

Fig.4.2.1 Device structure of OTFTs with bi-layer GeO/Au electrodes

4.3 Results and Discussion

Fig.4.3.1 (a) and (b) shows the output characteristics (V_D - I_D) of the OTFTs with only-Au and with 5 nm GeO, respectively. It is clearly seen that the drain current is highly increased in the device with 5 nm GeO, suggesting the formation of a good Ohmic contact. Fig.4.3.2 shows the transfer characteristics of the device with only-Au and with 5 nm GeO. The transfer characteristics were measured in the saturation regime with a source-drain voltage of V_D = ī 15. The device with 5 nm GeO also shows little improvement in threshold voltage and on/off ratio.

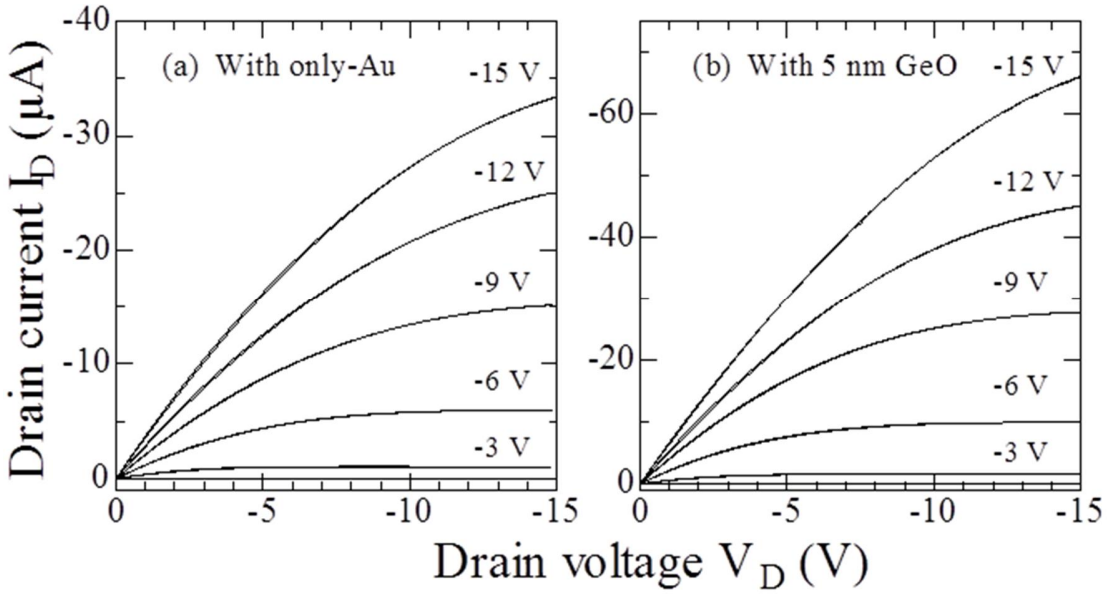

Fig.4.3.1 Drain current vs drain voltage characteristics of pentacene based OTFTs. (a) with only-Au and (b) with 5 nm GeO.

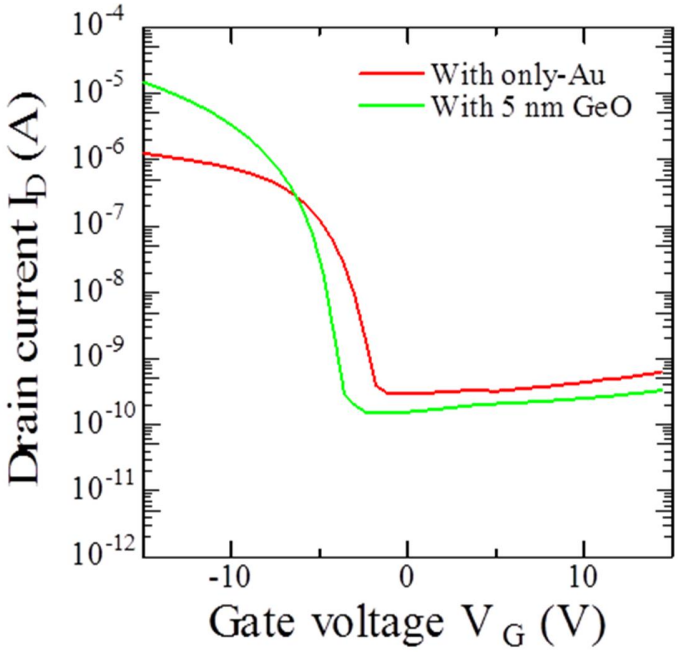

Fig.4.3.2 Transfer characteristics of pentacene based OTFTs corresponding to only-Au and with 5 nm GeO.

The field-effect mobility was estimated in the saturation region using the following equation as

$$I_D = \left(\frac{W}{2L}\right)\mu C_{OX}\left(V_G - V_T\right)^2. \quad (4.3.1)$$

Where, W and L are the channel width and length respectively, C_i is the gate dielectric capacitance per unit area, V_G and I_D are the gate voltage and drain current, respectively. The threshold voltages and on/off ratio were extracted from (V_G - I_D) characteristics. The device characteristics including field-effect mobility (μ), threshold voltage (V_T) and on/off ratio (I_{On}/I_{Off}) with varied thickness of GeO is summarized in Table 4.3.I. It can be clearly seen that the electrical performance in terms of μ, VT and on/off ratio of the devices with GeO bilayer electrodes was better than the device with only Au electrode. The devices with 5nm GeO shows the best performance with highest field effect mobility μ of 0.96 $cm^2\ V^{-1}s^{-1}$, V_T of -4V and the highest I_{On}/I_{Off} ratio of 5.2×10^4. The nature of OTFTs with an optimized 5 nm GeO is further investigated.

GeO Thickness (nm)	Mobility (cm^2/Vs)	Threshold voltage (V)	On/Off ratio ($\times 10^4$)
0	0.45	-0.5	1.5
2	0.62	-1.0	3.6
5	0.96	-4.0	5.2
10	0.81	-0.5	4.5
20	0.54	1.0	2.8

Table 4.3.I. Device characteristics varied with GeO thickness

Fig.4.3.3 (a) and (b) shows the temperature dependence of I_D-V_D curves in two devices with only-Au and with 5nm GeO, respectively. The I_D-V_D characteristics showed strong temperature dependence in both devices.

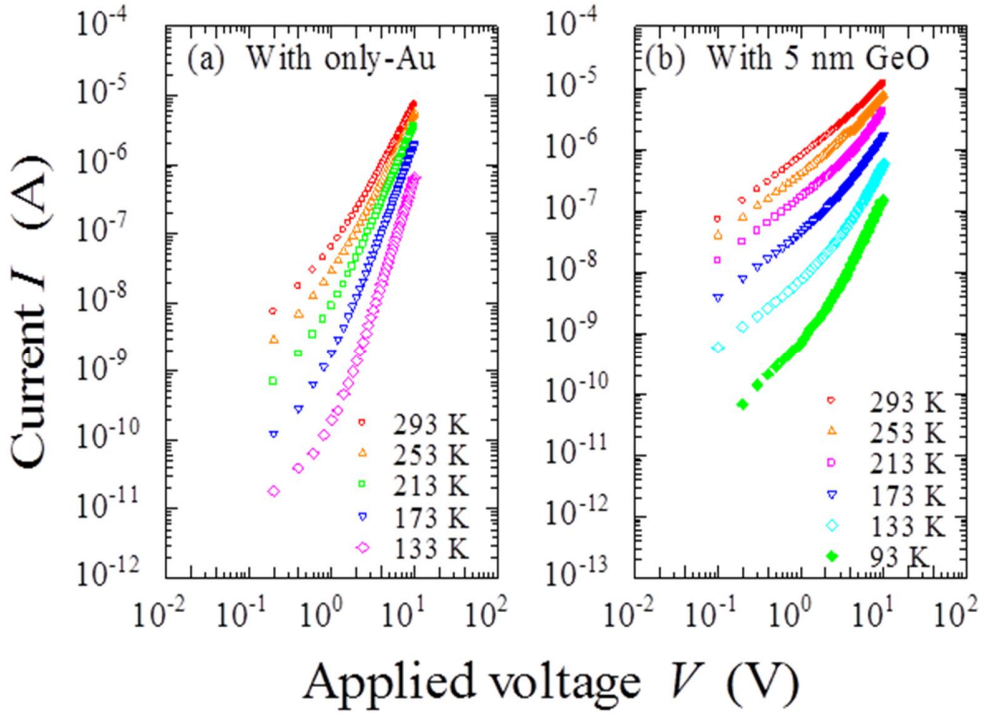

Fig.4.3.3 Temperature dependence of I_D-V_D characteristics of pentacene based OTFTs. (a) only-Au and (b) with 5 nm GeO.

In general, there are two possible injection mechanisms for the interface of metal/organic layer, i.e., Schottky thermionic emission and tunneling [9, 10]. The obvious temperature dependence of I_D-V_D curves in two devices suggests that the charge injection characteristics can be fitted by the Schottky emission mechanism which is discussed in detail elsewhere [11, 12]. By plotting the relationship between lnI vs $V^{1/2}$ and extrapolating straight lines to the ordinal point, the current at zero voltage I_0 is determined. By using the values of I_0, the relationship between lnI_0/T^2 vs $1/T$ is

plotted as shown in Fig.4.3.4 (a) and (b). From the resulting slope of extrapolated lines, the barrier heights of 0.12 eV and 0.01 eV were obtained corresponding to the case of only-Au and with 5 nm GeO, respectively. We can see that the barrier height was dramatically reduced by inserting 5 nm GeO between the Au and pentacene layer.

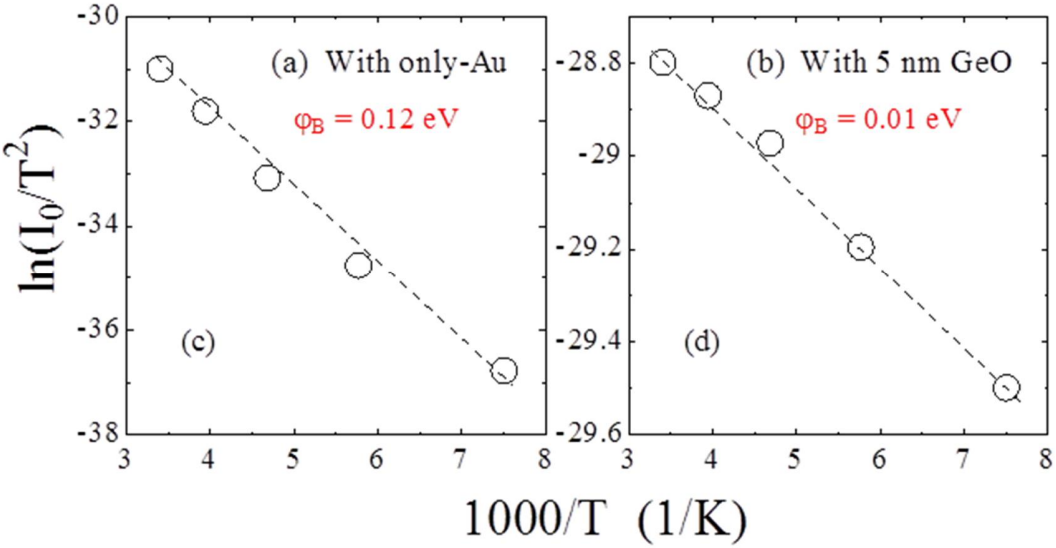

Fig.4.3.4 Relationship between$\ln(I_0/T^2)$ and $1/T$. (a) without and (b) with 5 nm GeO layer.

Fig.4.3.5 (a) and (b) shows the AFM micrograph of only pentacene layer and with 5 nm GeO, respectively. The root mean square (rms) roughness for both devices with only pentacene layer and with 5 nm GeO is 5.95 nm and 5.21 nm, respectively. It is clearly seen that with 5 nm GeO layer the surface of pentacene become more smooth which might be beneficial for achieving good Ohmic contacts. Noticeably, in the case of 2 nm thin GeO, the pentacene surface was not fully covered, and for 10 nm or thick GeO, the morphology of pentacene was completely eliminated and the new morphology of GeO was observed (micrograph not shown here).

Therefore, 5 nm GeO is enough for guaranteeing the fully covered pentacene layer until there was no direct connection between the active layer and the Au electrodes..

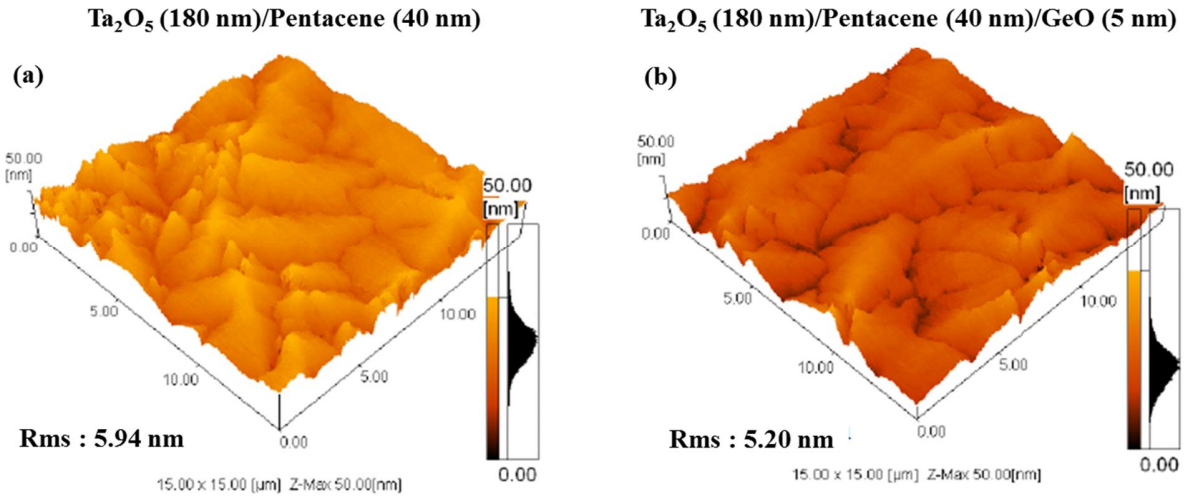

Fig.4.3.5 AFM images of pentacene films for (a) with only pentacene layer and (b) with 5 nm GeO.

Fig.4.3.6 shows the energy level diagrams for Au, GeO and pentacene. The (HOMO) of pentacene and Au lie at 5.0 eV and 5.1 eV, respectively [13, 14]. Germanium (Ge) metal has a high work function of around 4.7 eV and GeO has an electron affinity relative to Ge of around 2.7 eV and band gap of 2.8 eV [15, 16], which implies the valance band and conduction band position for GeO is located at 7.4 eV and 4.6 eV, respectively. Clearly the valence band position for GeO lies below the HOMO level of pentacene, resulting in no barrier for injection of holes into the pentacene layer. In addition, after modifying the organic/metal interface by inserting a thin layer of GeO, the source drain electrodes do not directly contact with pentacene layer which minimizes the penetration of the Au layer into the pentacene layer and provides a protection against the thermal diffusion of metal into the active layer, which avoids unfavorable chemical

reactions between organic and metal electrode. Therefore, it is easily understood that the barrier height and contact resistance at Au/pentacene interface is significantly reduced after inserting 5 nm GeO, which enhances the charge injection and device performance.

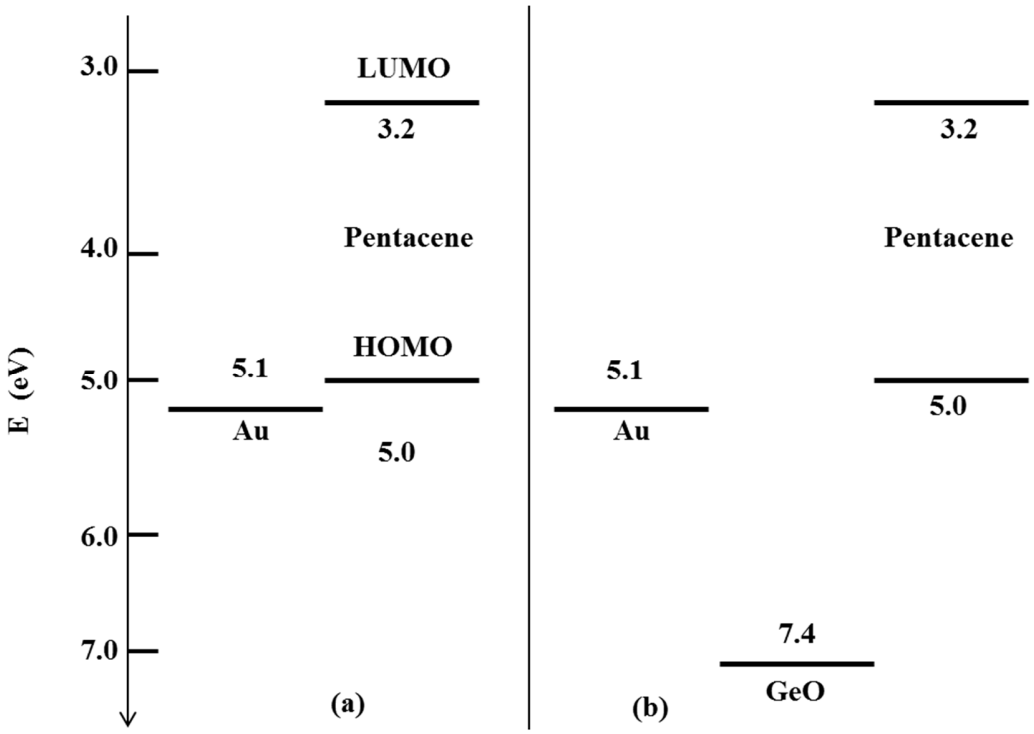

Fig.4.3.6 A schematic energy level diagram for (a) with only Au and pentacene interfaces and (b) with 5 nm GeO.

4.4 Conclusion

In conclusion, a top contact pentacene based OTFTs with bi-layer GeO/Au electrodes was investigated. The performance of the device after modification was highly improved and the highest mobility of 0.96 $cm^2 V^{-1}s^{-1}$, threshold voltage of -2 V and highest on/off ratio of 5.2×10^4 was achieved in the device with 5 nm GeO. The main factor for the improvement in the performance of the OTFTs with bi-layer GeO/Au electrodes was explained in terms of the

reduction in barrier height and smoothed surface roughness of active layer. Therefore, the combination of a thin 5 nm GeO with Au as a bi-layer electrode is an effective way to improve the characteristics of OTFTs which makes the device suitable for commercial applications.

4.5 References

[1] J. H. Cho, D. H. Kim, Y. Jang, W. H. Lee, K. Ihm, J. H. Han, S. Chung and K. Cho: Appl. Phys. Lett. **89**, 132101, 2006.

[2] S. D. Wang, T. Minari, T. Miyadera, K. Tsukagoshi and Y. Aoyagi: Appl. Phys. Lett. **91**, 203508, 2007.

[3] N. J. Watkins, L. Yan, and Y. Gao: Appl. Phys. Lett. **80**, 4384, 2002.

[4] N. Koch, J. Ghijsen, J. J. Pireaux, J. Schwartz, R. L. Johnson, A. Elschner, and A. Khan: Appl. Phys. Lett. **82**, 70, 2003.

[5] C. W. Chu, S. H. Li, C. W. Chen, V. Shrotriya and Y. Yang, Appl. Phys. Lett. **87**, 193508, 2005.

[6] M. W. Alam, Z. Wang, S. Naka and H. Okada: J. Photopolym. Sci. Tech. **25**, 659, 2012.

[7] P. Darmawan, T. Minari, A. Kumatani, Y. Li, C. Liu,and K. Tsukagoshi: Appl. Phys. Lett. **100**, 013303, 2012.

[8] J. W. Park, K. J. Baeg, J. Ghim, S. J. Kang, J. H. Park and D. Y. Kim: Electrochemical and Solid-State Lett. **10**, H340, 2007.

[9] S. Naka, M. Tamekawa , T. Terashita, H. Okada, H. Anada and H. Onnagawa: Synth. Met. **91**, 129, 1997.

[10] I. D. Parker: J. Appl. Phys. **75**, 1656, 1994.

[11] Y. Lou, Z. Wang, S. Naka and H. Okada: Appl. Phys. Lett. **99**, 033305, 2011.

[12] Z. Wang, M. W. Alam, S. Naka and H. Okada: Appl. Phys. Lett. **100**, 043302, 2012.

[13] Q. J. Sun, Z. Xu, S. L. Zhao, F. J Zhang, L. Y. Gao and Y. S. Wang: Synth. Met. **160**, 2239, 2010.

[14] Shen, G. Zhu, W. Guo, C. Tao, X. Zhang, C. Liu, W. Chen, S. Ruan and Z. Zhong: Appl. Phys. Lett. **92**, 073307, 2008.

[15] J. A. Dillon and H.E. Farnsworth: Phys. Lett. **28**, 174, 1956.

[16] S. Fadida, M. Eizenberg, L. Nyns, S. V. Elshocht and M. Caymax: Microelectronic Eng. **88**, 1557, 2011.

Chapter 5

Performance Enhancement of Top-Contact Pentacene-Based Organic Thin-Film Transistors with Bilayer WO_3/Au Electrodes

We fabricated top-contact pentacene-based organic thin-film transistors (OTFTs) with bilayer WO_3/Au electrodes. Compared with those of a device without a WO_3 layer, the performance characteristics including field-effect mobility, threshold voltage, and On/Off ratio were highly improved in a device with a 5nm WO_3 hole injection layer inserted. The field-effect mobility was increased from 0.47 to 0.69 $cm^2 V^{-1}s^{-1}$ and the On/Off ratio was also increased from $1:8\times10^4$ to $4:1\times10^4$. From the results of evaluating the temperature dependence of I_D–V_D characteristics and the surface morphology of pentacene, the improved device performance was attributed to reductions in barrier height and surface roughness after inserting a suitable WO_3 layer between the pentacene and gold electrodes.

5.1 Introduction

Nowadays, organic thin-film transistors (OTFTs) are widely used as driving elements for displays and logic circuits because of their envisioned applications in flexible, large area, low-cost, and light weight organic electronics, such as smart cards, identification tags, chemical sensors, and biochips [1ï 3]. Several studies on OTFTs revealed that the device performance is significantly improved through improvements in the device structure and fabrication techniques [4ï 8]. The performance of the OTFTs is highly dependent on the chosen semiconductor and dielectric materials. Pentacene is widely used as a semiconductor material owing to its high field-effect mobility [9, 10]. In particular, the performance of pentacene-based OTFTs is highly

dependent on the surface properties of the dielectric layer, such as surface roughness, and pentacene deposition conditions. By controlling the surface roughness of the dielectric material and the deposition conditions of pentacene, a large grain size and a high mobility could be achieved [11,12]. For constructing high-performance top-contact OTFTs, it is very important to understand the effect of metal diffusion into the organic film on its electrical performance. The metal diffusion mostly increases the contact resistance and limits the performance of the device [13ï 15]. To improve the hole injection and reduce the contact resistance at the organic/metal interface, a thin transition metal oxide layer is usually introduced between the metal electrode and the pentacene layer. It was also reported that hole mobility and current On/Off ratio were optimized after inserting a thin layer of V_2O_5, MoO_3, copper phthalocyanine (CuPc), or TiO_2 between the organic semiconductor and metal electrodes, owing to energy barrier reduction and an improved hole injection [16ï 20]. Among all transition metal oxides, tungsten oxide (WO_3) has excellent electrical, structural, and optical properties, which have attracted much attention in recent years [21, 22]. Because of its high work function, barrier-lowering properties, and charge generation abilities, WO_3 is often used as a hole injection layer in organic light-emitting diodes (OLEDs) and solar cells [23, 24]. Li et al. [25] and Cheung et al. [26] reported that the contact resistance in OTFTs can be reduced by inserting a WO_3 layer between the source/drain electrodes and the organic semiconductor. In this study, the main parameters that we investigated are the barrier height at the organic/ metal interface determined by evaluating the temperature dependence of drain current versus drain voltage (I_D–V_D) characteristics, and the surface morphology of pentacene. In this study, top-contact pentacene-based OTFTs were investigated by introducing WO_3 layers of different thicknesses between Au electrode and a pentacene layer

to study the temperature dependence characteristics and estimate the barrier height. As a result, the hole mobility and the drain current were highly increased by inserting a 5 nm WO_3 layer. The surface morphology of the pentacene/WO_3 films was also characterized by atomic force microscopy (AFM).

5.2 Experimental Details

A schematic diagram of top-contact pentacene-based OTFTs is shown in Fig.5.2.1. The devices were fabricated by using a cleaned glass substrate, which was ultrasonically cleaned in acetone, organic alkalies, and deionized water (18 Mq) successively and then dried using an air gun. Subsequently, 50-nm-thick tantalum (Ta) as gate electrode and 180-nm thick tantalum oxide (Ta_2O_5) as a gate insulator were deposited by RF sputtering. Following the sputtering of the gate insulator, 40-nm-thick pentacene (Sigma-Aldrich, 98% purity) was thermally evaporated at a low deposition rate of 0.15 ºA/s. During the deposition of pentacene, the substrate temperature was maintained at 60°C. Finally, WO_3 and 60-nm-thick gold were thermally evaporated onto the pentacene film through a metal mask to form the source/drain contacts with a channel length and width of 250 μm and 1 mm, respectively. The thickness of WO_3 was varied to 2, 5, and 10 nm. All thermal evaporations were performed under a pressure of less than $2\times10^{\bar{1}6}$ Torr. For comparison, a similar device without a WO_3 layer was also fabricated under the same conditions. Electrical measurements were performed at room temperature using a semiconductor parameter analyzer (HP 4155B). The I_D–V_D curves with varying temperature were measured to investigate carrier transport properties by loading the fabricated devices into a cryostat. The temperature was

varied from 93 to 293K by introducing a flow of liquid nitrogen into the sample holder in the vacuum chamber. The surface morphology of pentacene films was evaluated by AFM.

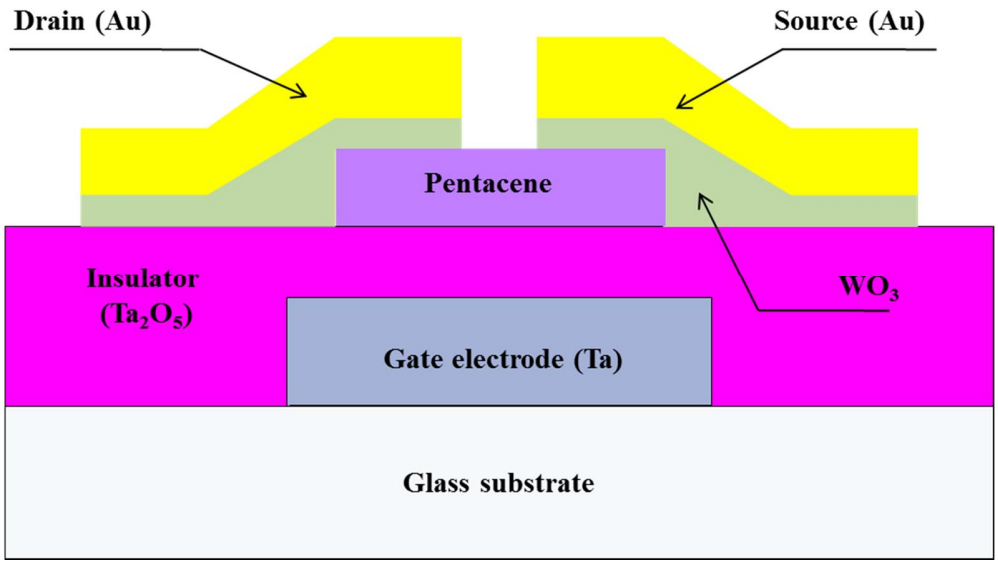

Fig.5.2.1 Structure of organic thin-film transistor with bilayer WO_3/Au electrodes.

5.3 Results and Discussion

Fig.5.3.1 (a) - (d), shows the V_D–I_D characteristics of the top contact pentacene-based OTFTs without and with 2, 5, and 10 nm WO_3 layers, respectively. For all devices, V_D ranged from 0 to -15 V and gate voltage (V_G) varied from 0 to 15 V. Fig.5.3.2 shows the transfer characteristics of all the devices without and with 2, 5, and 10 nm WO_3 layers. V_G was varied from 15 to -15V with a fixed V_D at -15 V. The field-effect mobility was estimated in the saturation region using

$$I_D = \left(\frac{W}{2L}\right)\mu\, C_{OX}\left(V_G - V_T\right)^2. \quad (5.3.1)$$

Where, W and L are the channel width and length respectively. Moreover, C_{OX} is the insulator capacitance per unit area (22.7 nF/cm^2), and V_G and V_T are the gate and threshold voltages respectively.

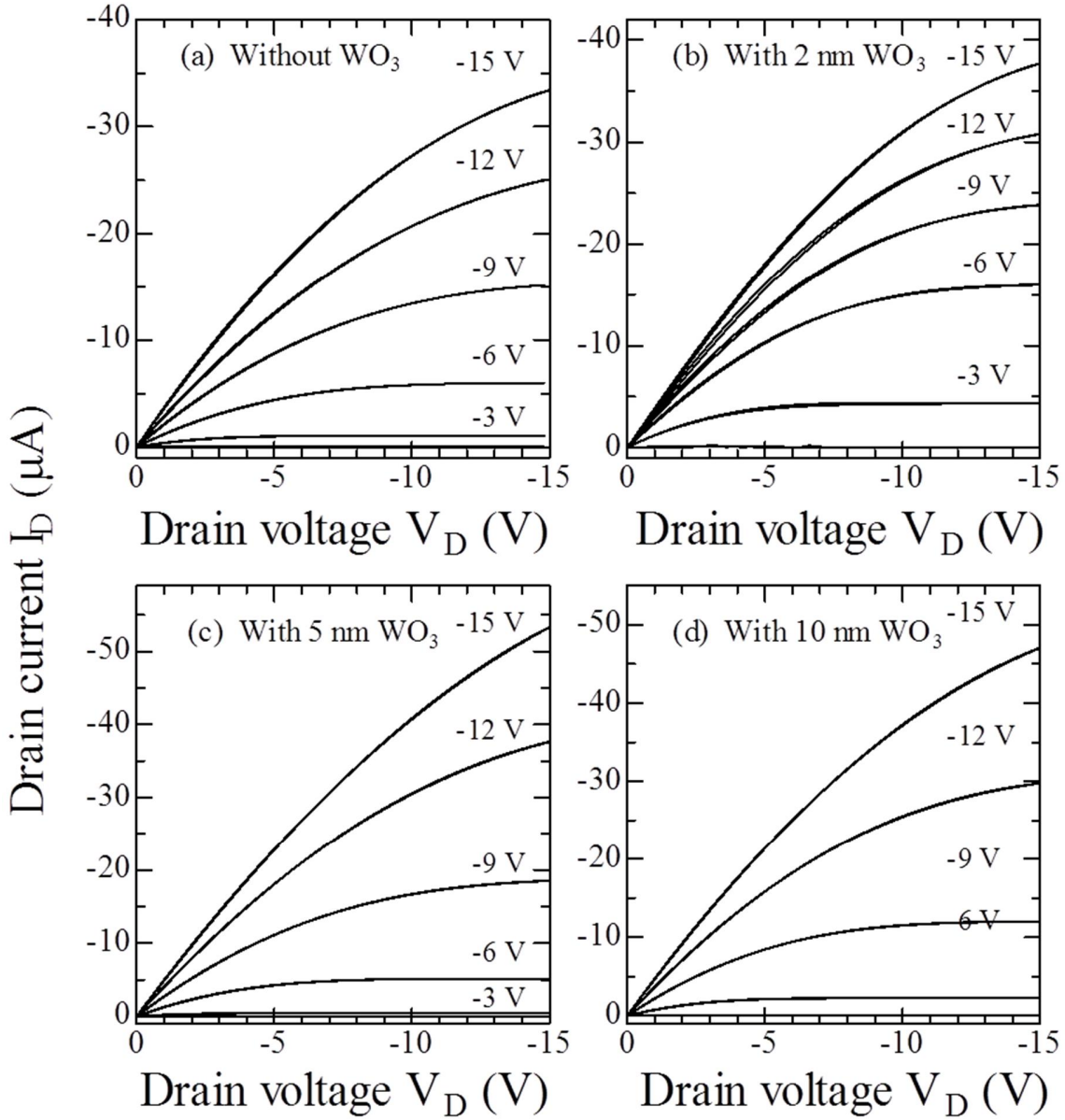

Fig.5.3.1 Drain current vs. drain voltage characteristics of OTFTs: (a) Without and with (b) 2, (c) 5, and (d) 10 nm WO_3 layers.

After inserting a 5 nm WO_3 layer, the field-effect mobility became 0.69 $cm^2\ V^{-1}s^{-1}$, which is the highest value among all the devices. The threshold voltage (V_{Th}) decreased from -0.5 to -2 V and the highest on/off ratio of $4.1\times10^4$was obtained.

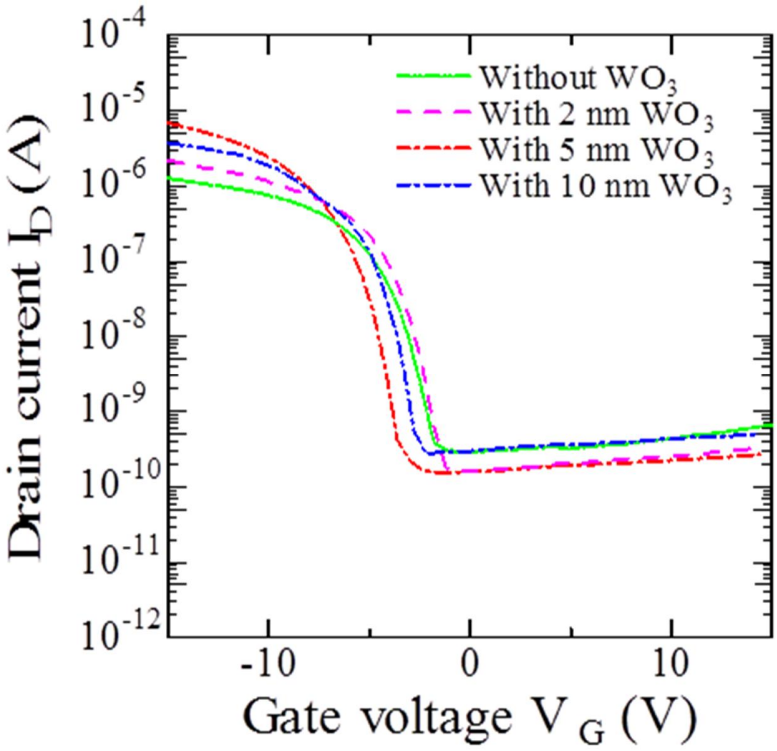

Fig.5.3.2 Transfer characteristics of OTFTs without and with 2, 5, and 10 nm WO_3 layers.

The sub threshold slope (S), which describes the turn on of the OTFTs, is also an important parameter in the device performance and is defined by

$$S = \frac{\partial V_G}{\partial(\log I_D)}. \quad (5.3.2)$$

The sub threshold slope is also derived from the transfer characteristics of the OTFTs.

The performance characteristics of all the devices with WO_3 layers of different thicknesses are shown in Table 5.3.1.

WO_3Thickness (nm)	**μ ($cm^2V^{-1}s^{-1}$)**	**V_{Th} (V)**	**S (V/dec)**	**On/off ratio**
0	0.47	-0.5	0.75	1.8×10^4
2	0.51	-0.5	0.65	2.4×10^4
5	0.69	-2	0.46	4.1×10^4
10	0.61	-1	0.74	3.1×10^4

Table 5.3.I. Device characteristics for various WO_3 thicknesses.

The minimum sub threshold slope of 0.46 V/decade is achieved in the device with a 5 nm WO_3 layer and the maximum slope of 0.75 V/decade is achieved in the device without a WO_3 layer. Threshold voltage is a figure of merit of the surface density of deeply trapped charges in both the channel and contact regions. Even though the WO_3 layer improves the hole injection, it may also create interfacial trap states at the interface. As a result, the trapped charges partially compensate the applied external field and shift the threshold voltage to become more negative. Pentacene films deposited by thermal evaporation have a polycrystalline nature, and the grain size and grain boundary density strongly affect the charge transport in the films. It is generally recognized that structural defects in pentacene films play an important role in electrical characteristics. The sub threshold slope is also one of the most important parameters of OTFTs and is mostly dominated by material properties, such as the grain size and grain boundary density of the pentacene layer [27]. After modification with a WO_3 layer, a change in the grain size of the pentacene layer is

observed, which may be a possible cause of the decrease in sub threshold slope. The small increase in On/Off ratio is mainly attributed to the better carrier injection after WO_3 modification, resulting in an increase in I_{On} while I_{Off} is almost invariable. By comparing the performance characteristics of all the devices, it is clear that the performance of the device with a 5nm WO_3/Au electrode was significantly improved by the large increase in drain current. The increase in drain current demonstrates that the hole injection from Au electrodes to pentacene was markedly improved by the increase in device mobility. When the thickness of the WO_3 layer is increased to 10 nm, the field-effect mobility and drain current decreased gradually. Therefore, the specific performance of OTFTs with the optimal 5 nm WO_3 layer was further investigated here.

The temperature dependence of I_D–V_D characteristics at a fixed gate voltage of 0 V was evaluated at temperatures between 133 and 293K. Fig.5.3.3 (a) and (b) shows the temperature dependence of I_D–V_D curves for both the devices without and with a 5 nm WO_3 layer, respectively. The I_D–V_D characteristics show strong temperature dependence in both devices. In general, there are two possible injection mechanisms for the interface of the metal/organic layer, i.e., Schottky thermionic emission and tunneling [28-30]. The obvious temperature dependence of I_D–V_D curves in the two devices suggests that the charge injection characteristics can be fitted by the Schottky emission mechanism as

$$I = A^{*}T^{2}\exp\left[\frac{-q\left(\varphi_B - \sqrt{qV/4\pi\varepsilon_i d}\right)}{kT}\right]. \quad (5.3.3)$$

Here, A* is the effective Richardson constant, T is the temperature, ϕB is the barrier height at the interface, q is the electronic charge, V is the applied voltage, "i is the dielectric permittivity, d is the thickness of the mixed single organic layer, and k is the Boltzmann constant.

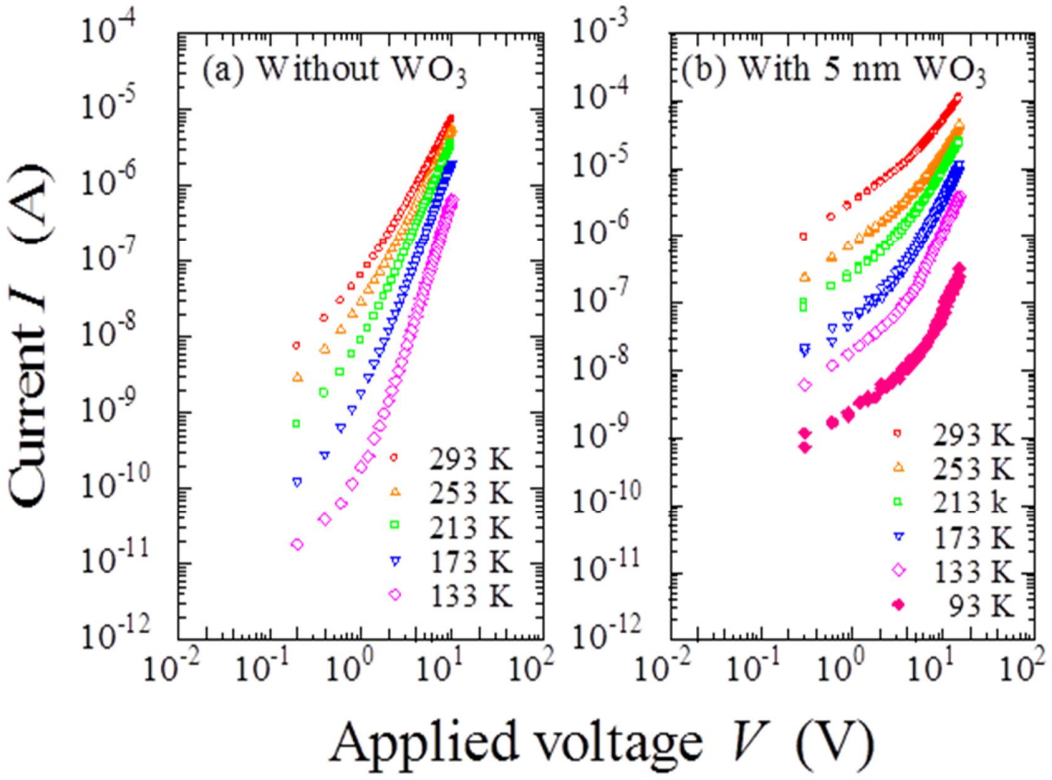

Fig.5.3.3 Temperature dependence of I_D-V_D characteristics (a) without and (b) with 5 nm WO_3 layer.

Fig.5.3.4 (a) and (b) show the *I–V* characteristics by plotting the relationship between *lnI* and $V^{1/2}$ and then extrapolating straight lines to the ordinal point, where the current at zero voltage I_0 is evaluated. The relationship between lnI_0/T^2 and $1/T$ is plotted in Fig.5.3.5 (a) and (b) using the values of I_0, resulting slopes of the extrapolated lines give the barrier heights of 0.12 and 0.05 eV at the pentacene/Au and pentacene/WO_3/Au interfaces, respectively. We can see that the barrier

height is markedly reduced by inserting a 5nm WO_3 layer between the organic and metal electrodes.

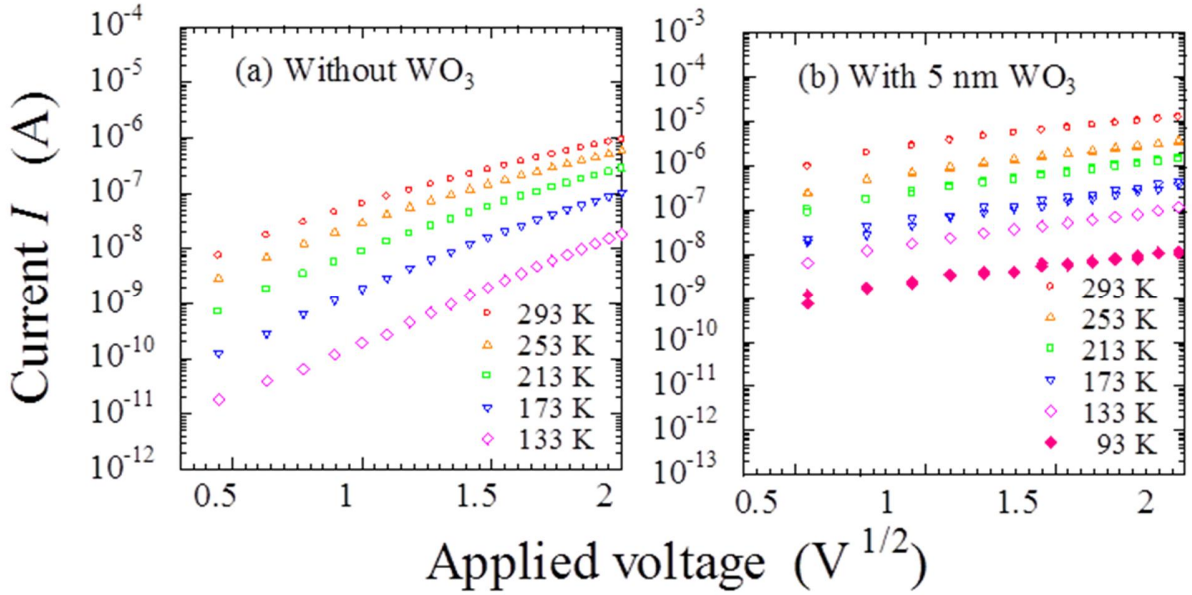

Fig.5.3.4 Relationship between lnI and $V^{1/2}$ (a) without and (b) with 5 nm WO_3 layer.

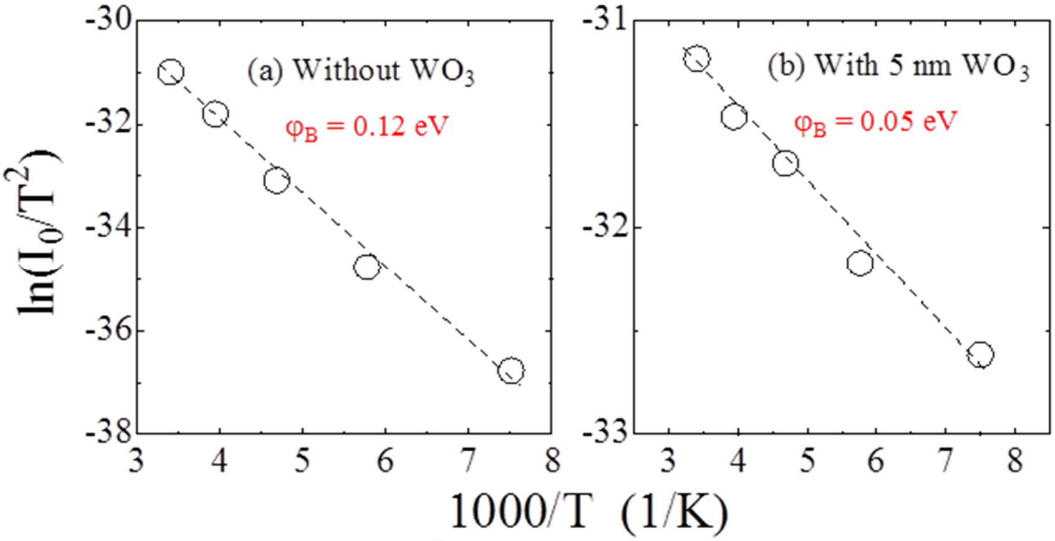

Fig.5.3.5 Relationship between $ln(I_0/T^2)$ and $1/T$. (a) Without and (b) with 5 nm WO_3 layer.

Fig. 5.3.6 (a) and (b) shows the AFM micrographs of the pentacene layers without and with a 5 nm WO_3 layer deposited on the Ta_2O_5 dielectric surface. The root mean square (RMS) roughnesses of both devices are 7.75 and 6.85 nm, respectively. With very thin WO_3 layers of 0 and 2 nm thicknesses, the pentacene layer is not fully covered and the morphology of pentacene remains unchanged (image not shown here). The performance of the OTFTs is highly dependent on the surface morphology of pentacene. A smoother pentacene surface is necessary to increase the charge injection and mobility [20, 28]. Clearly, the pentacene surface becomes smoother with the insertion of a 5 nm WO_3 layer, which is necessary for providing a better contact with metal electrodes. This is also one of the main reasons for reducing the barrier height and increasing the hole injection.

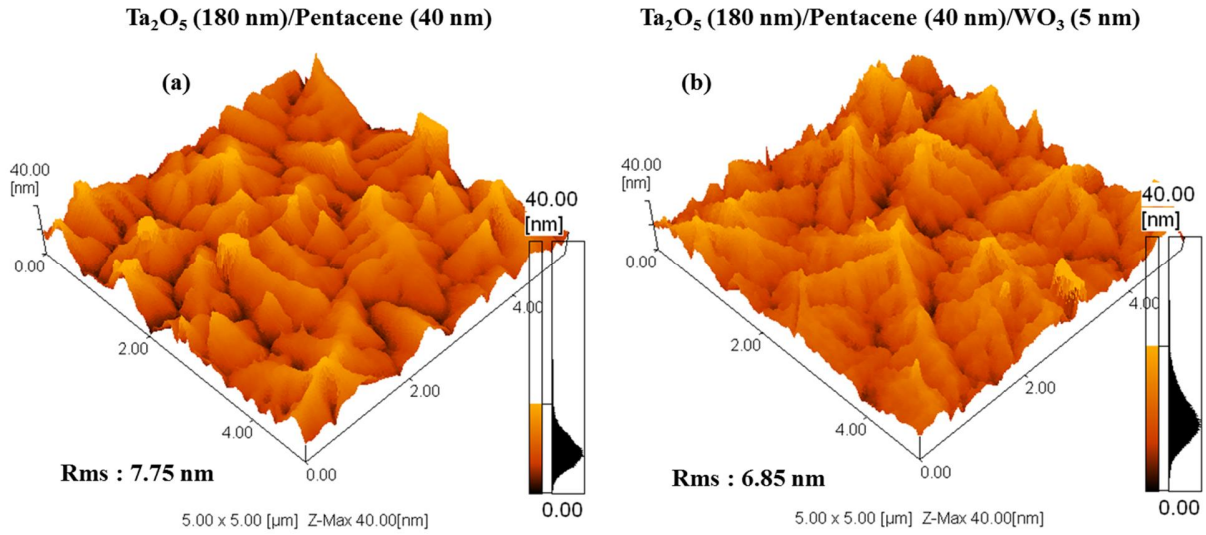

Fig. 5.3.6 AFM images of pentacene films (a) without and (b) with 5 nm WO_3 layer.

Cho et al. [31] reported that when a metal is directly deposited onto the pentacene layer, either it will penetrate into the upper layer of pentacene or diffuse into pentacene and form a mixture of

metal and pentacene in spite of using a pure metal. Therefore, an interface dipole barrier is formed, which shifts the highest occupied molecular orbital (HOMO) level of pentacene downward and increases the difference between the HOMO level of the pentacene layer and the Fermi level of the Au layer, which leads to a hole injection barrier of 1 eV [32, 33].

Fig.5.3.7 shows the energy level diagram of Au, pentacene, and WO_3. The work functions of pentacene, Au, and WO_3 lie at 5.0 [14], 5.1 [34] and 6.4 eV [35] respectively. The HOMO of pentacene adjusted with the valance band of WO_3 results in the absence of a barrier for the injection of holes into the pentacene layer.

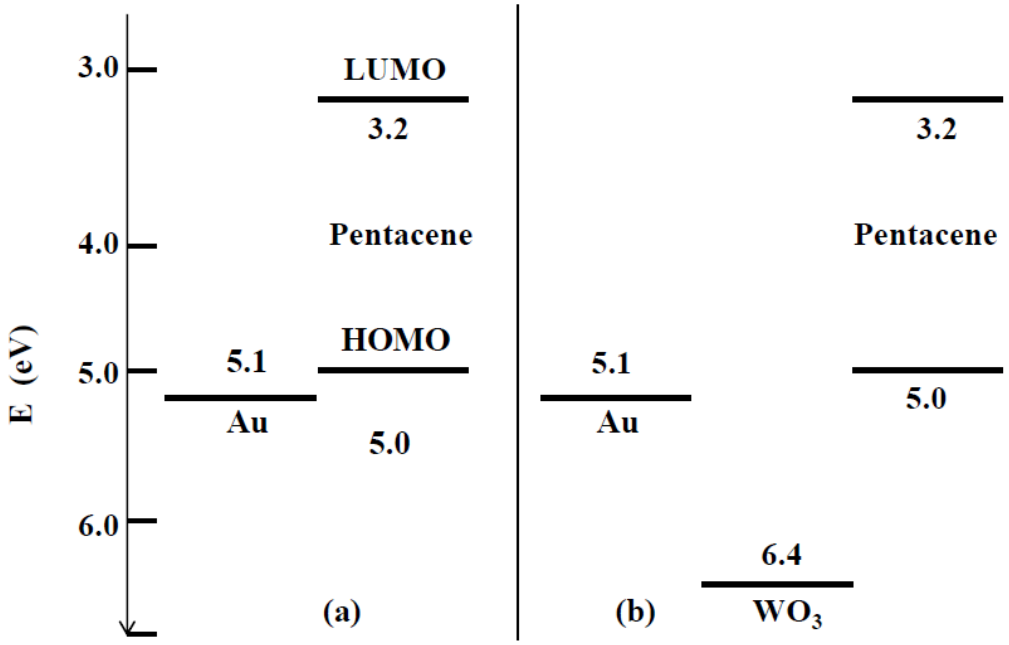

Fig.5.3.7 Energy level diagrams for Au, pentacene, and WO_3.

Therefore, by modifying the organic/metal interface through the insertion of a thin layer of WO_3, the source drain electrodes are not in direct contact with the pentacene layer, protecting the organic layer from metal penetration and preventing unfavorable chemical reactions between

organic and metal electrodes. For a thicker WO_3 layer of 10 nm, the contact resistance may be increased, which limits the device performance. Therefore, with an optimum intermediate WO3layer with a thickness of 5 nm, the active layer surfaces were fully covered and acted as blocking layers until there was no direct contact between the active layer and the Au electrodes. Therefore, it is easily understood that with the insertion of a WO_3 layer with a suitable thickness, the barrier height and contact resistance at the Au/pentacene interface decrease, resulting in enhanced charge injection and hence improved OTFT mobility.

5.4 Conclusion

We investigated pentacene-based OTFTs with WO_3 as a hole injection layer between metal electrodes and an organic semiconductor. By comparison it with that of the OTFT without a WO_3 layer, the performance of the device with a bilayer WO_3/Au electrode was observed to be significantly improved. The field-effect mobility increased from 0.47 to 0.69 cm^2 $V^{-1}s^{-1}$and the barrier height is also decreased from 0.12 to 0.05 eV with the insertion of a WO_3 layer. The improvement in the performance of the OTFTs is attributed to the decreased barrier height and reduced surface roughness after the insertion of the WO_3 layer. Therefore, using 5 nm WO_3 as the hole injection layer is an effective way to improve the characteristics of OTFTs, making the devices suitable for commercial applications.

5.5 References

[1] Z. Bao: Adv. Mater. **12**, 227, 2000.

[2] C. D. Dimitrakopoulos and P. R. L. Malenfant: Adv. Mater. **14**, 99, 2002.

[3] S. Liu, Q. Shen, Y. Cao, L. Gan, Z. Wang, M. L. Steigerwald and X. Guo: Coord. Chem. Rev. **254**, 1101, 2010.

[4] J. Park, S. I. Kang, S. P. Jang and J. S. Choi: Jpn. J. Appl. Phys. **44**, 648, 2005.

[5] T. Yokoyama, C. B. Park, K. Nagashio, K. Kita and A. Toriumi: Appl. Phys. Exp. **1**, 41801, 2005.

[6] S. Kang, J. Park, S. Jung, H. J. Lee, P. Son, J. C. Kim, T. H. Yoon and M. Yi: Jpn. J. Appl. Phys. **46**, 2696, 2007.

[7] F. Takeda, R. Sato, S. Naka and H. Okada: Jpn. J. Appl. Phys. **51**, 021604, 2012.

[8] T. Nagai, S. Naka, H. Okada and H. Onnagawa: Jpn. J. Appl. Phys. **46**, 2666, 2007.

[9] H. S. Seo, Y. S. Jang, Y. Zhang, P. S. Abthagir and J. H. Choi: Org. Electron. **9,** 432, 2008.

[10] D. Braga and G. Horowitz: Adv. Mater. **21**, 1473, 2009.

[11] A. L. Deman, M. Erouel, D. Lallemand, M. P. Goutorbe, P. Lang and J. Tardy: J. Non-Cryst. Solids **354**, 1598, 2008.

[12] J. H. Park, C. H. Kang, Y. J. Kim, Y. S. Lee and J. S. Choi: Mater. Sci. Eng. **C 24**, 27, 2004.

[13] Y. Bai, X. Liu, L. Chen, K. Haq, M. A. Khan, W. Q. Zhu, X. Y. Jiang and Z. L. Zhang: Microelectron. J. **38**, 1185, 2007.

[14] Q. J. Sun, Z. Xu, S. L. Zhao, F. J. Zhang, L. Y. Gao and Y. S. Wang: Synth. Met.**160**, 2239, 2010.

[15] S. D. Wang, T. Minari, T. Miyadera, K. Tsukagoshi and Y. Aoyagi: Appl. Phys. Lett. **91**, 203508, 2007.

[16] M. Minagawa, S. Kitamura, A. Baba, K. Shinbo, K. Kato and F. Kaneko: Appl. Phys. Exp. **2**, 071502, 2009.

[17] D. Kumaki, T. Umeda and S. Tokito: Appl. Phys. Lett. **92,** 013301, 2008.

[18] S. Tokito, K. Noda and Y. Taga: J. Phys. D **29**, 2750, 1996.

[19] F. C. Chen, L. J. Kung, H. T. H. Chen and Y. S. Lin: Appl. Phys. Lett. **90**, 073504, 2007.

[20] M. W. Alam, Z. Wang, S. Naka and H. Okada: J. Photopolym. Sci. Technol. **25,** 659, 2012.

[21] C. Y. Su and H. C. Lin: J. Phys. Chem. C **113**, 4042, 2009.

[22] F. Wang, C. Di Valentin and G. Pacchioni: J. Phys. Chem. C **115**, 8345, 2011.

[23] J. Meyer, M. Kroger, S. Hamwi, F. Gnam, T. Riedl, W. Kowalsky and A. Kahn: Appl. Phys. Lett. **96**, 193302, 2010.

[24] C. Tao, S. Ruan, G. Xie, X. Kong, L. Shen, F. Meng, C. Liu, X. Zhang, W. Dong and W. Chen: Appl. Phys. Lett. **94**, 043311, 2009.

[25] J. Li, X. W. Zhang, L. Zhang, K. Haq, X. Y. Jiang, W. Q. Zhu and Z. L. Zhang: Semicond. Sci. Technol. **24**, 115012, 2009.

[26] C. H. Cheung, K. K. Tsung, K. C. Kwok and S. K. So: Appl. Phys. Lett. 93, 083307, 2008.

[27] J. Park, Y. S. Jeong, K. S. Park, L. M. Do, J. H. Bae, J. S. Choi, C. Pearson and M. Petty: J. Appl. Phys. **111**, 104512, 2012.

[28] Z. Wang, M. W. Alam, S. Naka and H. Okada: Appl. Phys. Lett. **100**, 043302, 2012.

[29] S. Naka, M. Tamekawa, T. Terashita, H. Okada, H. Anada and H. Onnagawa: Synth. Met. **91**, 129, 1997.

[30] I. D. Parker: J. Appl. Phys. **75**, 1656, 1994.

[31] H. Cho, D. H. Kim, Y. Jang, W. H. Lee, K. Ihm, J. H. Han, S. Chung and K. Cho: Appl. Phys. Lett. **89**, 132101, 2006.

[32] N. J. Watkins, L. Yan and Y. Gao: Appl. Phys. Lett. **80**, 4384, 2002.

[33] N. Koch, J. Ghijsen, J. J. Pireaux, J. Schwartz, R. L. Johnson, A. Elschner and A. Khan: Appl. Phys. Lett. **82**, 70, 2003.

[34] L. Shen, G. Zhu, W. Guo, C. Tao, X. Zhang, C. Liu, W. Chen, S. Ruan and Z. Zhong: Appl. Phys. Lett. **92**, 073307, 2008.

[35] J. Meyer, S. Hamwi, T. Bu¨low, H.-H. Johannes, T. Riedl and W. Kowalsky: Appl. Phys. Lett. **91**, 113506, 2007.

Chapter 6

Temperature Dependence of Barrier Height and Performance Enhancement of Pentacene Based Organic Thin Film Transistor with Bi-Layer MoO_3/Au Electrodes

We investigated top-contact pentacene-based organic thin-film transistor (OTFTs) with bi-layer MoO_3/Au electrodes. The device performance including field effect mobility, threshold voltage, and On/Off ratio was highly improved in a device with 5 nm MoO_3 layer which shows highest field-effect mobility of 0.72 $cm^2 V^{-1}s^{-1}$. In addition, from temperature dependence characteristics we observed that the barrier height was dramatically decreased from 0.12 eV (without MoO_3) to 0.03 eV in device with 5 nm MoO_3 layer. This improved device performance was attributed to significant reduction in barrier height at Au/pentacene interfaces and surface roughness of pentacene layer after inserting a suitable MoO_3 layer between pentacene and gold electrodes.

6.1 Introduction

In recent years, organic thin-film transistors (OTFTs) have received much attention due to their potential applications in displays, logic circuits and also promising applications to flexible and low cost electronic devices, such as smart cards identification tags, and sensors [1-4]. From the performance point of view, the most important parameters are field effect mobility (μ), threshold voltage (V_T), sub threshold slope (S) and On/Off ratio (I_{on}/I_{off}). Pentacene has been widely used as the active layer in OTFTs due to their high field-effect mobility which is comparable to that of amorphous Si and till now several numbers of techniques have been used to improve the performance of pentacene-based OTFTs [5-8]. Up to date, higher mobility in OTFTs based on

polycrystalline films has been demonstrated using pentacene as organic semiconductor layer. The larger grain size and improved mobility for pentacene could be achieved by either decreasing the dielectric surface roughness or by modifying the pentacene deposition conditions and post-deposition treatments. For constructing a high performance top-contact OTFTs, it is important to understand the influence of the metal diffusion into the organic film on its electrical performance. When metal is directly deposited onto organic layer, diffusion between the organic layer and metal may be occurred. Chu et al. [9] shows that the contact between the source-drain electrodes and the organic semiconductor can be improved by using a transition metal oxide layers. Modification of organic/metal interface becomes an efficient way to reduce the electron injection barrier between the organic active layer and the metal electrodes. Molybdenum oxide (MoO_3), with diverse structural, optical, hole injection and charge generation abilities [10-12] have attracted much attention in recent years and is highly used in organic devices as a hole transporting layer [13-15]. The main parameter that we investigated in this study was the temperature dependence characteristics of barrier height and the surface morphology of pentacene layer.

In this study, we introduced MoO_3 interlayer of different thickness between the pentacene and Au electrodes and investigated the role of MoO_3 on the device performance of top-contact pentacene-based OTFTs. We observed that by inserting an appropriate MoO_3 layer between the pentacene and Au electrodes, the barrier height and surface roughness was highly decreased which enhance the device performance.

6.2 Experimental Details

A schematic structure of the top-contact pentacene-based OTFT upon investigation was shown in Fig.6.2.1. The devices were fabricated using cleaned glass substrate, on which 50 nm thick tantalum (Ta) as gate electrode and 180 nm tantalum oxide (Ta_2O_5) as gate dielectric were deposited by radio-frequency sputtering. After that, 40 nm pentacene (Sigma-Aldrich,98% purity) layer was evaporated with slow deposition rate of 0.15 Å/s through a metal mask. The substrate temperature was kept at 60 °C during deposition. Finally, MoO_3 with varied thickness and Au (60 nm) were evaporated onto the pentacene layer by using a metal mask to form the source and drain electrodes. The channel length and width was 250 µm and 1 mm, respectively. The thickness of MoO_3 was varied as 0, 2, 5 and 10 nm.

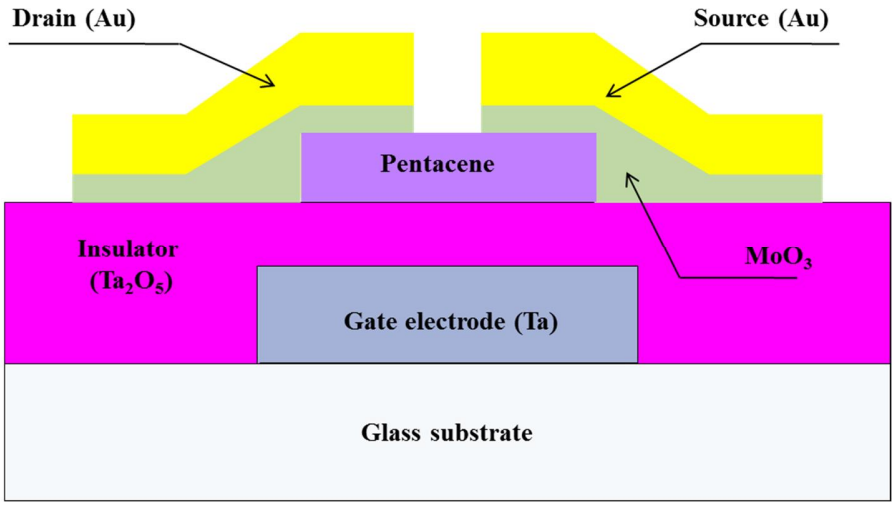

Fig. 6.2.1 Structure of OTFTs with bilayer MoO_3/Au electrodes.

Electrical measurements were performed at room temperature using a semiconductor parameter analyzer (HP 4155B). The drain current Vs drain voltage (I_D-V_D) curves with varying temperature at a fixed gate voltage of 0 V are measured for investigation of carrier transport properties by loading the fabricated devices into a cryostat. The temperature was varied from 133

to 293 K by flowing liquid nitrogen into the sample holder in the vacuum chamber. The surface morphology of pentacene films were evaluated using atomic force microscopy (AFM).

6.3 Results and discussion

The field-effect mobility was estimated in the saturation region using the following equation as

$$I_D = \left(\frac{W}{2L}\right)\mu\, C_{OX}\left(V_G - V_T\right)^2. \quad (6.3.1)$$

where, W and L are the channel width and length respectively, C_i is the gate dielectric capacitance per unit area and V_G, I_D are the gate voltage and drain current, respectively. Fig.6.3.1 (a) and (b) shows the output characteristics (V_D - I_D) of the OTFTs without and with 5 nm MoO_3 layer, respectively. Both devices exhibit typical p-channel characteristics. Noticeably, the drain current in the device with 5 nm MoO_3 layer was largely enhanced compared with that of the non-modified device which means the hole injection from Au electrodes to pentacene was remarkably improved which enhances the device performance. Fig.6.3.2 shows the transfer characteristics of the device without and with 5 nm MoO_3 layer.

The sub threshold slope (S), which describes turn on of the OTFTs, is also one another important parameter for the device performance, and is defined by the following equation

$$S = \frac{\partial V_G}{\partial\left(\log I_D\right)}, \quad (6.3.2)$$

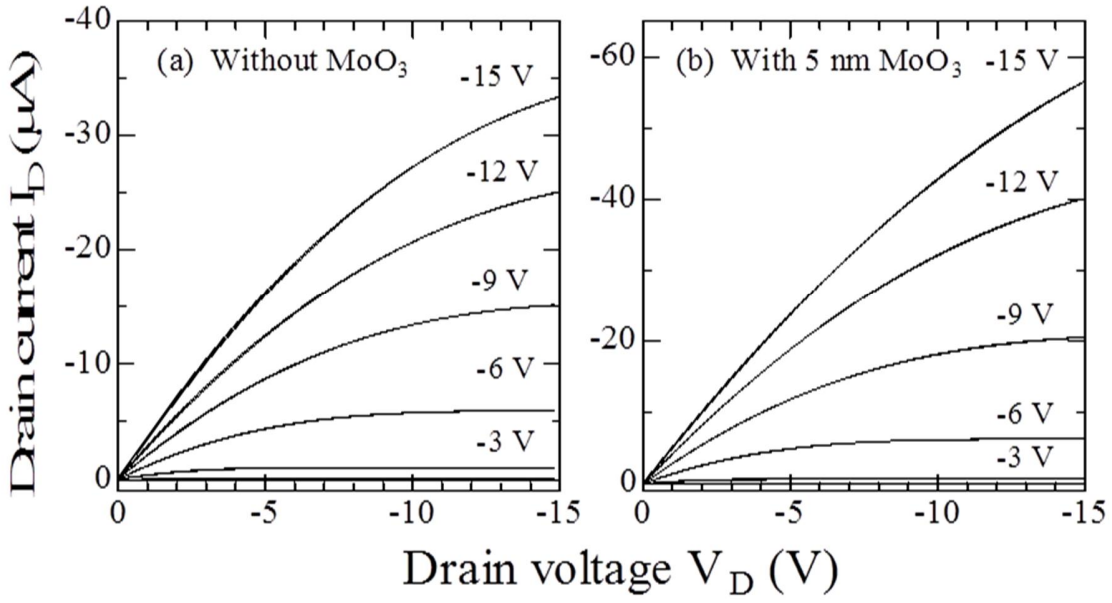

Fig.6.3.1 Drain current vs drain voltage characteristics of OTFTs. (a) with out and (b) with 5 nm MoO_3 layer.

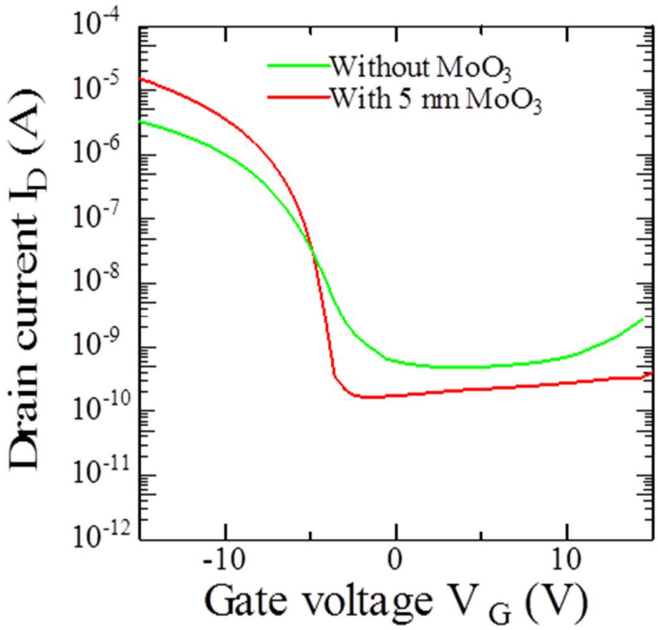

Fig.6.3.2 Transfer characteristics of OTFTs without and with 5 nm MoO_3 layer.

Threshold voltage, sub threshold slope and On/Off ratio was extracted from the transfer characteristics of the OTFTs at a source-drain voltage V_D = -15 V. The minimum sub threshold

slope of 0.49 V/decade was achieved in the device with 5 nm MoO_3 layer and maximum slope of 0.75 V/decade in the device without MoO_3 layer. The device characteristics including field-effect mobility, threshold voltage, Sub threshold slope and on/off ratio with varied thickness of MoO_3 is summarized in Table 6.3.1.The highest mobility of 0.72 $cm^2 V^{-1}s^{-1}$ and highest On/Off ratio of 4.3×10^4 is achieved in the device with 5 nm MoO_3 layer which is the higher values among all other devices. Meanwhile a little improvement in threshold voltage, sub threshold voltage after modification with 5 nm MoO_3 layer was also observed. Clearly among all the devices (without, with 2 nm, 5 nm and 10 nm MoO3 layer) the device with 5 nm MoO_3 layer shows best electrical characteristic. Therefore the specific performance of OTFTs with an optimized 5 nm MoO_3 layer was further investigated.

MoO_3 Thickness (nm)	**Mobility ($cm^2 V^{-1} s^{-1}$)**	**Threshold Voltage (V)**	**Sub threshold slope (V/dec)**	**On/Off ratio $\times10^4$**
0	0.47	-0.5	0.75	1.8
2	0.55	-0.5	0.68	2.6
5	0.72	-2.5	0.49	4.3
10	0.63	-1.0	0.73	3.4

Table.6.3.1 Device characteristics varied with MoO_3 thickness

Threshold voltage is a figure of merits of the surface density of deeply trapped charge both in channel and contact regions [16]. Therefore, it has a little decrease because the density of deeply trapped state is reduced after modification. In addition Even though by inserting MoO_3 layer the hole injection is improved, it may also create interfacial trap states on the interface. Which

results, the trapped charges partially compensate the applied external field and shift the threshold voltage to more negative. The sub threshold slope is mostly dominated by the material properties like grain size and grain boundary density of the pentacene layer [17]. After modification with MoO_3 layer the change in the grain size of pentacene layer is observed which may be the possible cause for the decrease in the sub threshold slope. The small increase in On/Off ratio is mainly attributed to better carrier injection after MoO_3 modification.

The temperature dependence of I_D-V_D characteristics was evaluated in the temperatures range between 133 and 293 K. Fig.6.3.3 (a) and (b) shows the temperature dependence of I_D-V_D curves in two devices without and with 5 nm MoO_3 layer, respectively. The I_D-V_D characteristics show strong temperature dependence in both the devices. In general, there are two possible injection mechanisms for the interface of metal/organic layer, i.e., Schottky thermionic emission [18-19] and tunneling [20]. The obvious temperature dependence of I_D-V_D curves in two devices suggests that the charge injection characteristics can be fitted by the Schottky emission mechanism.

$$I = A^{*}T^{2}\exp\left[\frac{-q\left(\varphi_B - \sqrt{qV/4\pi\varepsilon_i d}\right)}{kT}\right]. \quad (6.3.3)$$

where A* is the effective Richardson constant, T the temperature, φ_B the barrier height at the interface, q the electronic charge, V the applied voltage, ε_i the dielectric permittivity of the mixed organic layer, d the dielectric thickness, and k the Boltzmann constant. Fig.6.3.4 (a) and (b) shows the I-V characteristics by plotting the relationship between lnI vs $V^{1/2}$ and extrapolating straight lines to the ordinal point, the current I_0 is evaluated. By using the values of I_0 the

relationship between lnI_0/T^2 vs $1/T$ is plotted in Fig.6.3.5 (a) and (b). The resulting slope of extrapolated lines give the barrier heights of 0.12 eV and 0.03 eV are obtained corresponding to the case of without and with 5 nm MoO_3 layer respectively. We can see that the barrier height is dramatically reduced by inserting MoO_3 layer between the pentacene and metal electrodes.

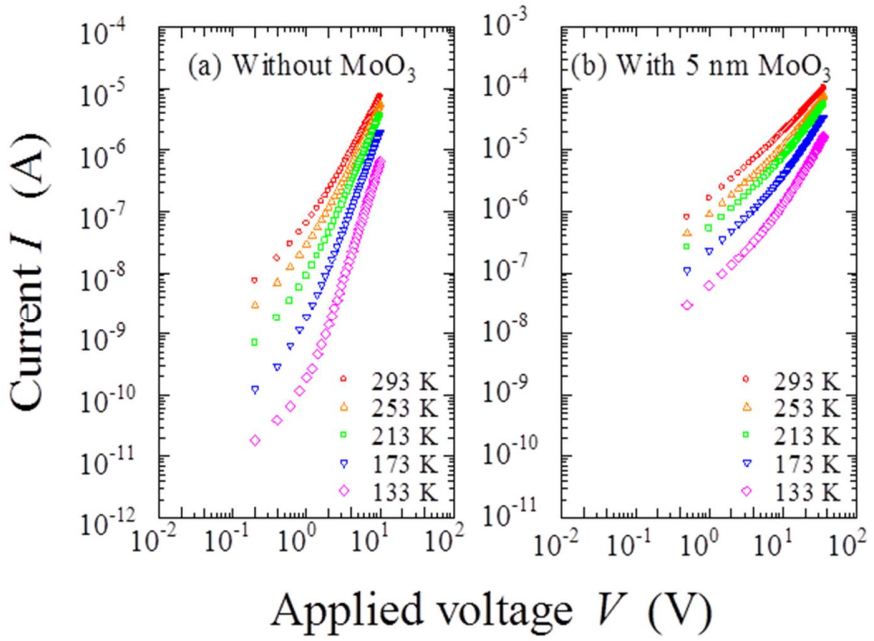

Fig.6.3.3 Temperature dependence I_D-V_D characteristics of the devices (a) without and (b) with 5nm MoO_3 layer .

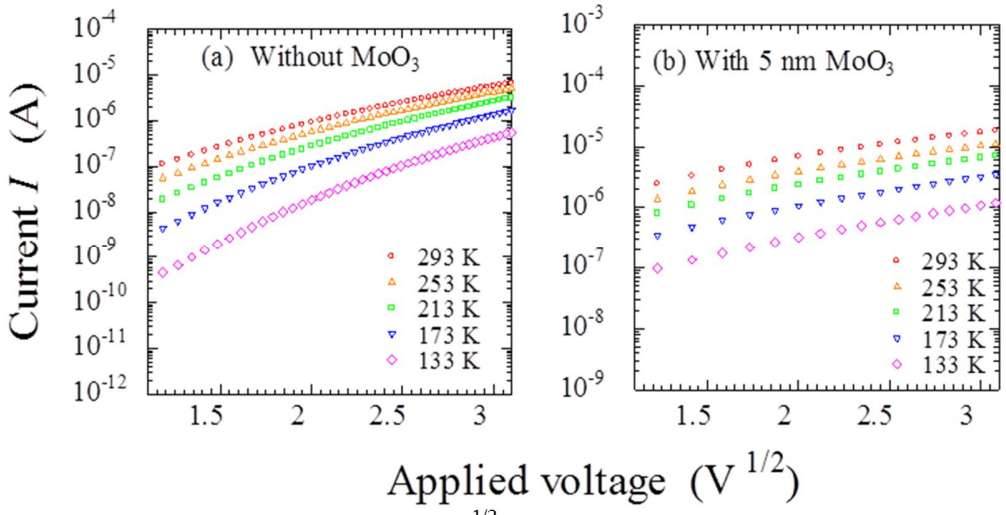

Fig.6.3.4 Relationship between lnI and $V^{1/2}$ (a) without and (b) with 5 nm MoO_3 layer.

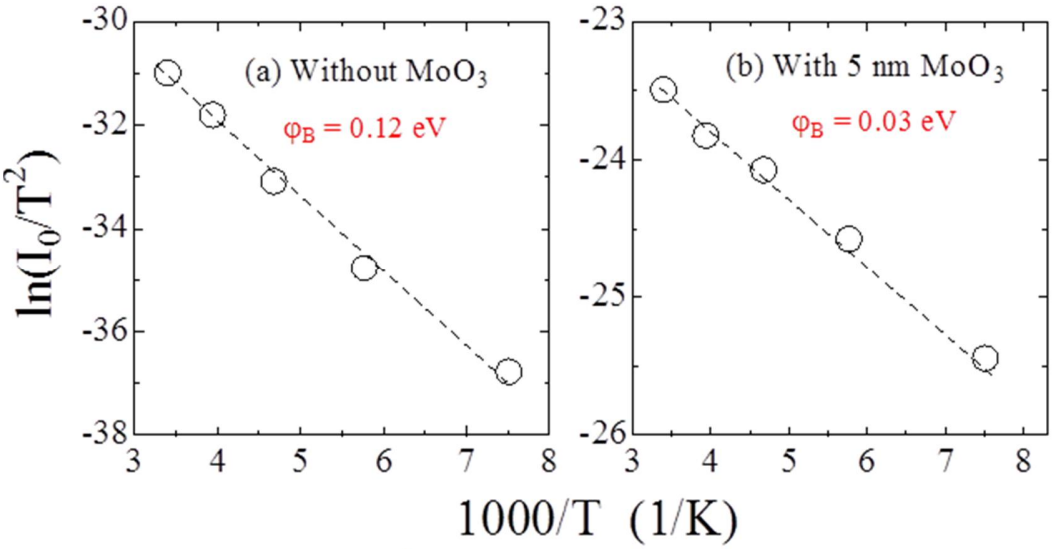

Fig.6.3.5 Relationship between $\ln(I_0/T^2)$ and $1/T$ corresponding to (a) without and (b) with 5 nm MoO_3 layer.

Fig.6.3.6 (a) and (b) show the AFM micrograph of pentacene layer with and without 5 nm MoO_3 layer, respectively. The root mean square (rms) roughness for both devices with out and with 5 nm MoO_3 is 4.55 nm and 4.07 nm, respectively. It is observed that with 2 nm thin MoO_3 layer the pentacene surface was not fully covered (micrograph not shown). For 10 nm or thick layer the new morphology of MoO_3 is observed while the morphology of pentacene was completely eliminated. D. W. Zhao et al [21] also shows that the thicker (10 nm) MoO_3 hole transporting layer increases the contact resistance which limits the device performance. Therefore, only with intermediate MoO_3 thickness (5 nm) the surfaces of the active layer were fully covered until there was no direct connection between the pentacene layer and the Au electrodes. The 5 nm MoO_3 could then act as a hole transporting blocking layer and the surface of pentacene becomes smoother in a certain extent which led to a significant increase in the performance of the device.

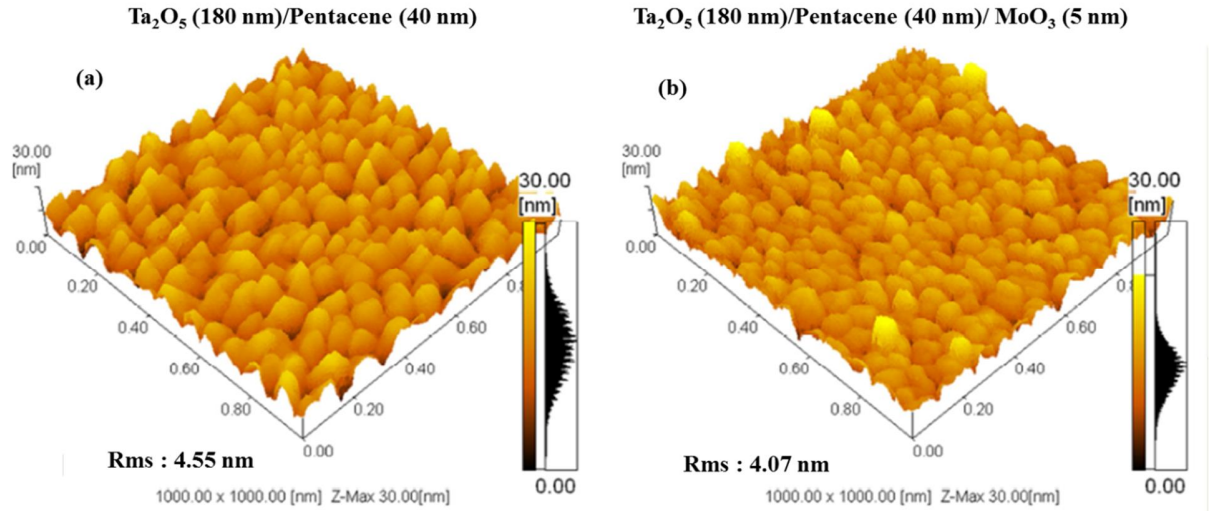

Fig.6.3.6 AFM images of pentacene films for (a) without and (b) with 5 nm MoO_3 layer.

In order to understand the detailed reasons for the improvement in the mobility and device performance it is very important to understand the contact interfaces between the metal electrodes and Pentacene. To achieve the Ohmic characteristics it is necessary that the work function of the metal is closer to the HOMO or LOMO of the organic materials, which lead to enhance the charge injection [9]. For Pentacene/Au contacts there is small mismatch between the work function of Au and HOMO level of pentacene which results to relatively high contact resistance at the Pentacene/Au interfaces. When a metal is directly deposited onto the pentacene, either it will penetrate into the upper layer of pentacene or diffuse into pentacene to form a mixture of metal and pentacene in spite of pure metal [22]. Therefore high contact resistance is observed resulting from the formation of interface dipole barrier which shifts the HOMO level of pentacene downward causing an increase in the difference between the HOMO level of the pentacene and the Fermi level of the Au, hence increasing the barrier height [23, 24]. The 5 nm MoO_3 layer minimize the penetration of the Au layer into the pentacene layer and provided a

protection against the diffusion of metal into the organic layer, which avoids unfavorable chemical reaction between organic and metal electrodes [10]. Fig.6.3.7 shows the energy level diagrams for Au, MoO_3 and pentacene. The highest molecular orbitalôs (HOMO) of pentacene, MoO_3 and Au lie at 5. 0 eV, 5.3 eV and 5.1 eV respectively [25, 26]. The HOMO of MoO_3 is much deeper than the Au and pentacene and aligned them with the HOMO level of pentacene which reduce the barrier height between the two layers. As the 5 nm MoO_3 layer was thermally evaporated therefore during evaporation MoO_3 may contain some impurities like MoO or free Mo which decrease the space-charge region between the metal and MoO_3 interfaces resulting in good Ohmic contacts and current flows very rapidly which reduce the contact resistance and therefore device mobility and performance is highly increased.

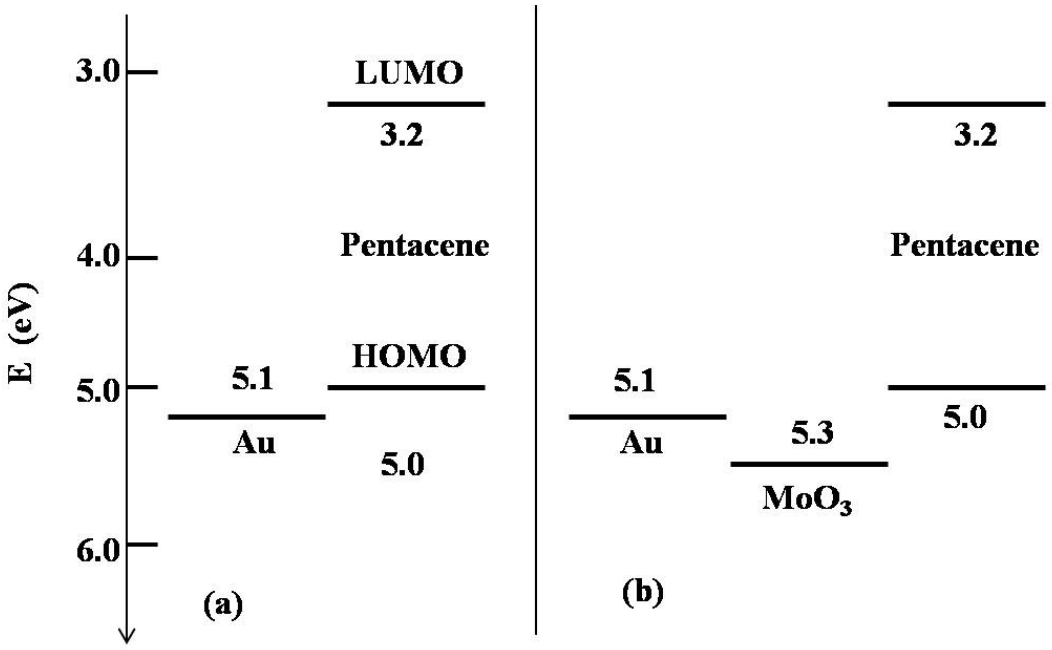

Fig.6.3.7 Energy level diagrams for Au, MoO_3 and Pentacene.

6.4 Conclusion

In summary, we have investigated a pentacene based OTFT by inserting 5 nm MoO3 layer between the Au and Pentacene layer. Compared with OTFTs without MoO3 layer, the drain current and the field-effect mobility were significantly improved. The field-effect mobility increased from 0.47 cm^2 $V^{-1}s^{-1}$ to 0.72 cm^2 $V^{-1}s^{-1}$ and threshold voltage is also decreased. By evaluating of the temperature dependence of I_D-V_D characteristics, the barrier height is dramatically decreased from 0.12 eV (with Au-only) to 0.03 eV in device with 5 nm MoO_3 layer. The lowered barrier height is attributed to the smoothed surface of pentacene with MoO_3 modification, which is confirmed by our AFM observation of pentacene surface morphology. Therefore Using MoO_3 the Au/pentacene interfaces as the hole injection layer is an effective way to improve the device performance.

6.5 References

[1] Z. Bao: Adv. Mater. **12**, 227, 2000.

[2] C. D. Dimitrakopoulos and P. R. L. Malenfant: Adv. Mater. **14**, 99, 2002.

[3] S.Liu, Q. Shen, Y. Cao, L. Gan, Z. Wang, M. L. Steigerwald and X. Guo: Coord. Chem. Rev. **254**, 1101, 2010.

[4] L. Torsi, N. Cioffi, C. Di Franco, L. Sabbatini, P. G. Zambonin and T. B. Zacheo: Solid-State electron. **45**, 1479, 2001.

[5] H. S. Seo, Y. S. Jang, Y. Zhang, P. S. Abthagir and J. H. Choi: Org. Electron. **9,** 432, 2008.

[6] D. Braga and G. Horowitz: Adv. Mater. **21**, 1473, 2009.

[7] H. Klauk, G. Schmid, W. Radlik, W. Weber, L. Zhou, C. D. Sheraw, J. A. Nichols and T. N. Jackson: Solid-State Electron. **47,** 297, 2003.

[8] M. Zhu, G. Liang, T. Cui and K. Varahramyan: Solid-State Electron. **49**, 884, 2005.

[9] C. W. Chu, S. H. Li, C. W. Chen, V. Shrotriya and Y. Yang: Appl. Phys. Lett. **87**, 193508, 2005.

[10] S. S. Mahajan, S.H. Mujawar, P.S. Shinde, A.I. Inamdar and P.S. Patil: Int. J. Electrochem. Sci. **3**, 953, 2008.

[11] A. K. Prasad, D. J. Kubinski and P. I. Gouma: Sensors and Actuators B. **93,** 25, 2003.

[12] T. S. Sian and G.B. Reddy: App. Surf. Sci. **236**, 1, 2004.

[13] X. Y. Jiang, Z. L. Zhang, J. Cao and W.Q. Zhu: Solid-State Electron. **52**, 952, 2008.

[14] R. Liu, C. Xu, R. Biswas, J. Shinar and R. Shinar: Appl. Phys. Lett. **99**, 093305, 2011.

[15] S. Tokito, K. Noda and Y. Taga: J. Phys. D **29**, 2750, 1996.

[16] Y. W. Wang and H. L. Cheng: Solid-State Electron. **53,** 1107, 2009.

[17] J. Park, Y. S. Jeong, K. S. Park, L. M. Do, J. H. Bae, J. S. Choi, C. Pearson and M. Petty: J. Appl. Phys. Lett. **111**, 104512, 2012.

[18] Y. Lou, Z. Wang, S. Naka and H. Okada: Appl. Phys. Lett. **99**, 033305, 2011.

[19] S. Naka, M. Tamekawa, T. Terashita, H. Okada, H. Anada and H. Onnagawa: Synth. Met. **91**, 129, 1997.

[20] I. D. Parker: J. Appl. Phys. **75**, 1656, 1994.

[21] D. W. Zhao, P. Liu, X. W. Sun, S. T. Tan, L. Ke and A. K. K. Kyaw: Appl. Phys. Lett. **95,** 153304, 2009.

[22] J. H. Cho, D. H. Kim, Y. Jang, W. H. Lee, K. Ihm, J. H. Han, S. Chung and K. Cho: Appl. Phys. Lett. **89**, 132101, 2006.

[23] N. J. Watkins, L. Yan and Y. Gao: Appl. Phys. Lett. **80**, 4384, 2002.

[24] N. Koch, J. Ghijsen, J.-J.Pireaux, J. Schwartz, R. L. Johnson, A. Elschner and A. Khan, Appl. Phys. Lett. **82**, 70, 2003.

[25] Q. J. Sun, Z. Xu, S. L. Zhao, F. J Zhang, L. Y. Gao and Y. S. Wang: Synthetic Met. **160**, 2239, 2010.

[26] L. Shen, G. Zhu, W. Guo, C. Tao, X. Zhang, C. Liu, W. Chen, S. Ruan and Z. Zhong: Appl. Phys. Lett. **92**, 073307, 2008.

Chapter 7

Top Contact Pentacene Based Organic Thin Film Transistor with Bi-layer TiO_2/Au Electrodes

We fabricated a Top contact Pentacene based Organic thin-film transistor (OTFTs) with bi-layer TiO_2/Au electrodes. The performance of the devices after inserting TiO_2 layer between organic layer and Au electrode is highly improved. On Comparing with Pentacene based transistor with only Au electrode the hole injection was largely enhanced and the highest field-effect mobility is increased from 0.37 to 0.63 cm^2 $V^{-1}s^{-1}$ in the device with bilayer TiO_2/Au electrodes. We also measured the temperature dependence characteristics and surface morphology of both the devices. Both the devices showed strong temperature dependence. We observed that the barrier height is tremendously decreased after inserting a thin layer of TiO_2 between the organic layer and Au electrodes. The improved device performance was due to the decreased barrier height and decrease in the surface roughness of pentacene after inserting a suitable metal oxide layer between the pentacene and the Au electrodes. Our experimental results clearly show that the insertion of metal oxide between Au electrode and pentacene layer is an effective way to improve the performance of the Pentacene based organic thin-film transistor (OTFTs).

7.1 Introduction

Organic thin-film transistors (OTFTs) have received considerable attention because of their envisioned applications in flexible, large area, low-cost and light weight organic electronics,

such as smart cards, identification tags, chemical sensors and biochips and are widely used as the driving elements for displays, logic circuits [1-3]. The performance of the OTFT is highly dependent on choosing the semiconductor and the dielectric materials. From the performance point of view, the most important parameters are charge carrier mobility, on/off current ratio and the operational voltage range. Currently, highest field effect mobility has been obtained with pentacene based organic thin film transistor [4, 5]. Particularly the performance of the pentacene based OTFT is highly dependent on the surface properties of dielectric layer and pentacene deposition conditions. By controlling the surface roughness of dielectric material and the deposition conditions of pentacene large grain size and high field effect mobility could be achieved [6, 7]. While constructing high-performance top-contact OTFTs, it is very important to understand the influence of interfaces which play a crucial role in the overall performance of the device. Mainly there are two kinds of interfaces in a transistor the first one is in between the semiconductor and the gate dielectric, where the conducting channel forms, and the second one is in between the source/drain electrodes and the semiconductor layer where charge carriers are injected. In this study we particularly discuss the latter one. Organic and metal interfaces mostly limit the performance of the device and field effect mobility is also decreased. In earlier reports it has been shown that the diffusion between the metal electrode and pentacene reduced the hole injection carrier at the interface which causes the increase in barrier height and contact resistance which effect the performance of the OTFTs [8-11]. Itôs been shown that the contact between the S-D electrodes and the organic semiconductor can be improved by inserting transition metal oxide layer as carrier injection layers. Because of good electronic properties, transition metal oxides offer a unique opportunity to control the work function, and hence increase the charge-

injection properties [12-15]. Therefore, by modifying the organic/electrode interface by inserting a thin layer of transition metal oxides, the source drain electrodes do not directly contact with pentacene layer and hence significantly reduces the contact resistance, barrier height and provides protection from diffusion and other chemical reactions which increases device performance. Among all the transition-metal oxides, TiO_2 is one of the most extensively studied materials because of their excellent structural, optical and electronic properties [16, 17]. Because of its high work function [18, 19] and electron accepting and conducting abilities Titanium dioxide (TiO_2) is highly used in metal-oxide/polymer photovoltaic devices [20-24].

In this paper we fabricated the top contact pentacene based OTFT by inserted a thin layer of TiO_2 as hole injection layer between the Au electrodes and organic layer. We found that by inserting a thin layer of transition metal oxides between metal electrodes and pentacene layer significantly reduced the barrier height and protect the device from diffusion which increases the device performance.

7.2 Experimental details

The schematic diagram of top contact pentacene based OTFTs with bilayer TiO_2/Au electrodes is shown in Fig.7.2.1. The devices were made by using cleaned glass substrate which was ultrasonically cleaned in acetone, semicoclean and deionized water (18 Mq) consecutively and then dried by air gun. After washing a 50 nm thick tantalum (Ta) as gate electrode and 180 nm tantalum oxide (Ta_2O_5) as gate insulator were deposited by RF sputtering. Then a 40-nm-thick layer of pentacene (Sigma-Aldrich, 98% purity) was thermally evaporated with slow deposition rate of 0.15 Å/ s. during deposition of pentacene the substrate temperature was kept at 60 °C.

Finally, TiO_2, and 60 nm Au were thermally evaporated onto the pentacene film through a metal mask to form S / D contacts with a channel length and width of 250 µm and 1 mm respectively. The thickness of TiO_2 was varied from 2, 5 and 10 nm. All thermal evaporations were done under a pressure of less than 2×10ī 6 Torr. For comparison a similar device under same conditions with Au-only electrode (Without TiO_2 layer) was also fabricated.

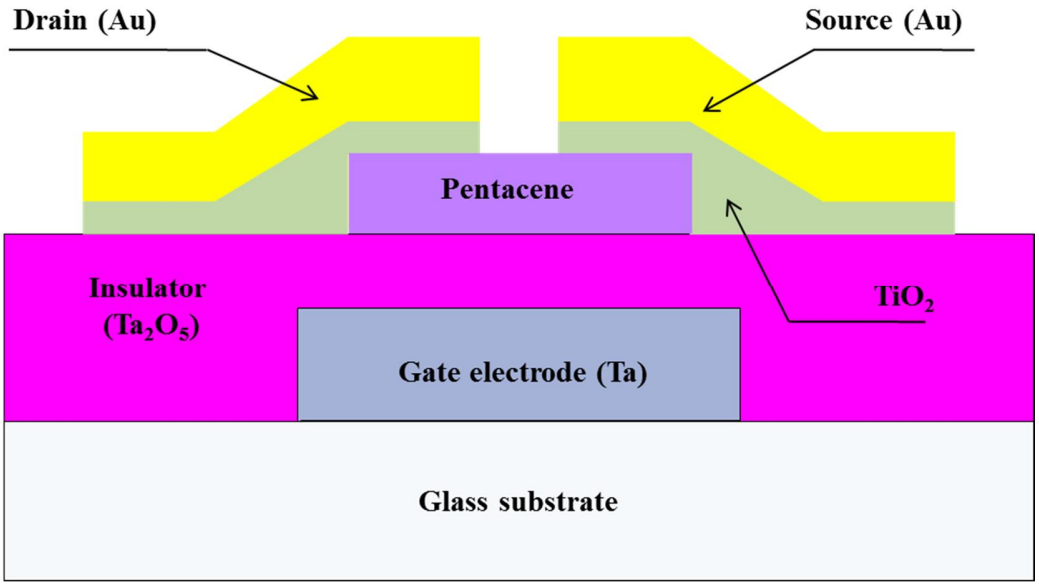

Fig.7.2.1.Structure of organic thin film transistor with bilayer TiO_2/Au electrodes.

Electrical measurements were performed at room temperature using HEWLETT PACKARD 4155B semiconductor parameter analyzer. The drain current Vs drain voltage (I_D-V_D) curves with varying temperature are measured for investigation of carrier transport properties by loading the fabricated devices into a cryostat. The temperature is varied from 93 to 293 K by flowing liquid nitrogen into the sample holder in the vacuum chamber. The surface morphology of pentacene films were evaluated using atomic force microscopy (AFM).

7.3 Results and discussions

The output characteristics (V_D-I_D) of the top contact pentacene-based OTFTs with only Au, and with 5 nm TiO_2, layer were shown in Fig.7.3.1 (a) and (b), respectively. For all devices source/drain voltages (V_D) ranged from 0 to -15 V and gate voltages (V_G) were varied from 0 to -15 V.

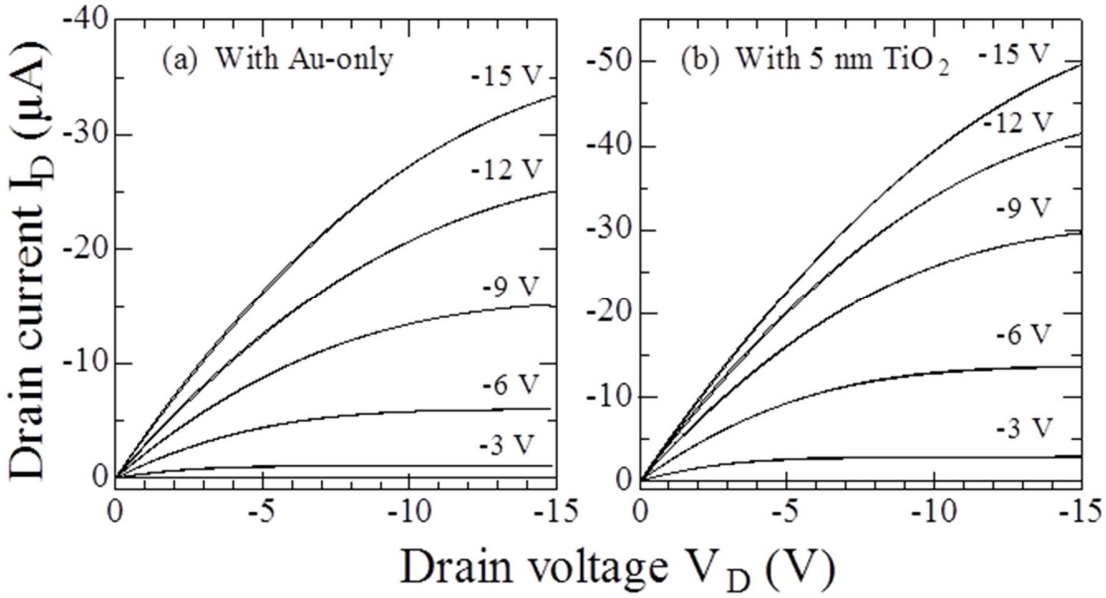

Fig.7.3.1 Drain current Vs Drain voltage characteristics of OTFTs. (a) With Au-Only and (b) with 5 nm TiO_2 layer

Fig.7.3.2 shows the transfer characteristic (V_G - I_D) of the devices with, TiO_2 and only Au electrodes. The gate voltage V_G was varied from 15 V to -15 V with a fixed sourceï drain voltage V_D at -15 V. The field-effect mobility was estimated in the saturation region using the following equation as

$$I_D = \left(\frac{W}{2L}\right)\mu\, C_i\left(V_G - V_T\right)^2. \quad (7.3.1)$$

Where I_D is the drain current, W and L are the channel width and channel length respectively, C_i is the insulator capacitance per unit area (22.7 nF/cm^2) and V_G and V_T are the gate and threshold voltage, respectively.

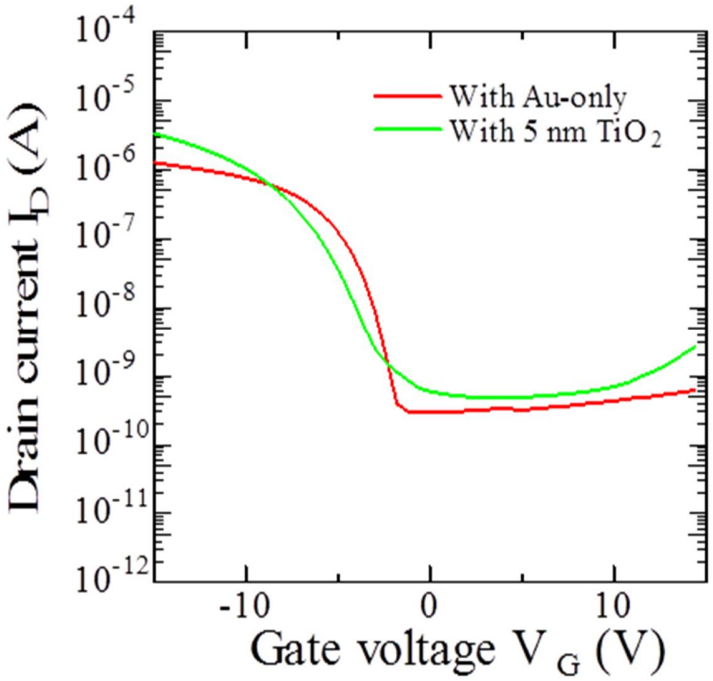

Fig.7.3.2 Transfer characteristics of OTFTs with Au-Only and with 5 nm TiO_2 layer

We found that the highest output current and field-effect mobility of 0.63 cm^2 V^{-1}s^{-1} can be achieved in the device with 5 nm TiO_2 bilayer electrodes, which is higher than that of the device with only Au electrode with mobility of 0.37 cm^2 V^{-1}s^{-1}. There is also little improvement in the threshold voltage and On/Off ratio. The threshold voltage is decreased from -0.3 V to -1.5 V and the highest On/Off ratio (about 3.7×10^4) is obtained from the device with 5 nm TiO_2 layer. The performance of all the devices with different thickness of TiO_2 is shown in table 7.3.1.

TiO_2 Thickness (nm)	μ (cm^2/Vs)	V_T (V)	I_{On}/I_{Off}
0	0.37	-0.3	1.8×10^4
2	0.49	-0.5	2.6×10^4
5	0.63	-1.5	3.7×10^4
10	0.52	-1.0	3×10^4

Table.7.3.1 Device characteristics varied with TiO_2 thickness.

On comparing the performance of the device with different thickness of TiO_2 and with only Au electrodes, itôs clearly seen that the performance of the device with only 5 nm TiO_2/Au electrodes is significantly improved. In addition, it is shown that the drain current was largely enhanced only with 5 nm TiO_2 layer between Au and pentacene. It is supposed that with a very thin transition metal oxide layer 0-4 nm the active layer may not be fully covered and hence the pentacene layer is not protected well. For a thicker TiO_2 layer of around 10 nm increase the contact resistance and barrier height and caused the mismatch of optical field distribution in active layer, which resulted in a decrease in the performance of the device. Therefore, only with intermediate TiO_2 layer with thickness (5 nm) the surfaces of the active layer were fully covered until there was no direct connection between the active layer and the Au electrodes. The TiO_2 could then act as a hole transporting blocking layer, which led to a significant increase in the performance of the device. The surface of TiO_2 can be easily modified with many organic

materials. This may increase the charge carrier efficiency at the interface between organic layer and Au electrodes. It is supposed that the TMOs layer provided a protection against the diffusion of metal into the organic layer, which avoids unfavorable chemical reaction between organic and metal electrodes. The insertion of blocking layer resulted in some changes at the interface of Au/pentacene and hence the device performance is improved.

In order to understand the detailed mechanism, temperature dependence of I_D-V_D characteristics were investigated over a wide temperature range of 93K-293K. Fig.7.3.3 (a) and (b) shows the temperature dependence of I_D-V_D curves.

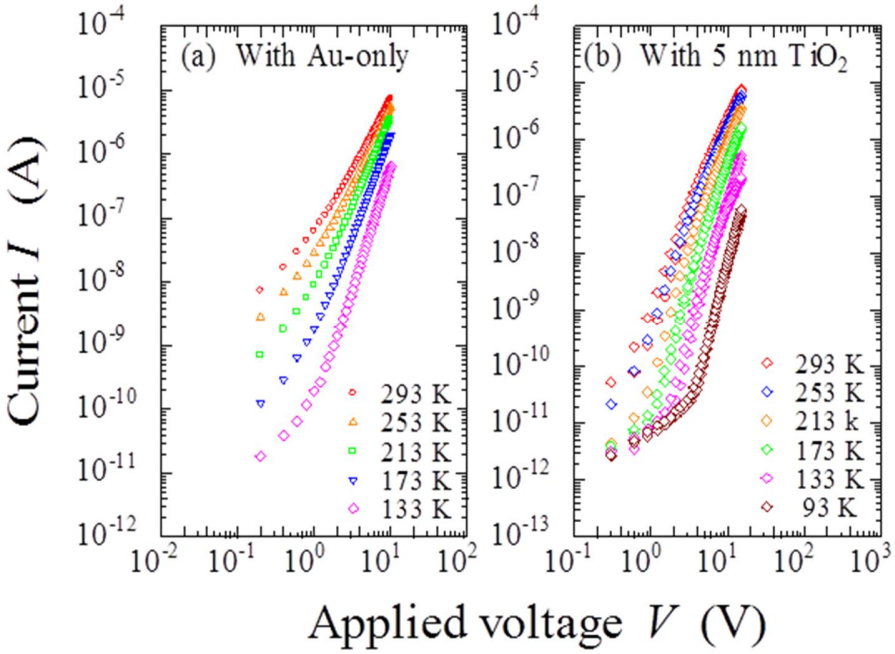

Fig.7.3.3 The temperature dependence I_D-V_D characteristics: With Au-Only and (b) with 5 nm TiO_2 layer

In general, there are two possible injection mechanisms for the interface of metal/organic layer, i.e., Schottky thermionic emission [25-26] and tunneling [27]. As the I_D-V_D characteristics show

strong temperature dependence in both the devices therefore the carrier-injection is explained by thermionic (Schottky) emission mechanisms.

$$I = A^{*}T^{2}\exp\left[\frac{-q\left(\varphi_{B} - \sqrt{qV/4\pi\varepsilon_{i}d}\right)}{kT}\right]. \quad (7.3.2)$$

where $A^{*}$is the effective Richardson constant, T the temperature, φB the barrier height at the interface, q the electronic charge, V the applied voltage, εi the dielectric permittivity of the mixed organic layer, d the thickness of mixed single organic layer, and k the Boltzmann constant. By plotting the relationship between lnI vs $V^{1/2}$ and extrapolating straight lines to the ordinal point, the current at zero voltage I_0 is evaluated. Using the values of I_0 the relationship between lnI_0/T^2 vs $1/T$ is plotted as shown in Fig.7.3.4 (a) and (b),We observed that the barrier height is dramatically reduced by inserting TiO_2 layer between the organic and metal layers. Therefore, it is easily understood as following: with insertion of suitable thickness of TiO_2, barrier height and contact resistance at the interface of Au/pentacene is reduced, which results in enhanced charge injection and then improved mobility of OTFTs.

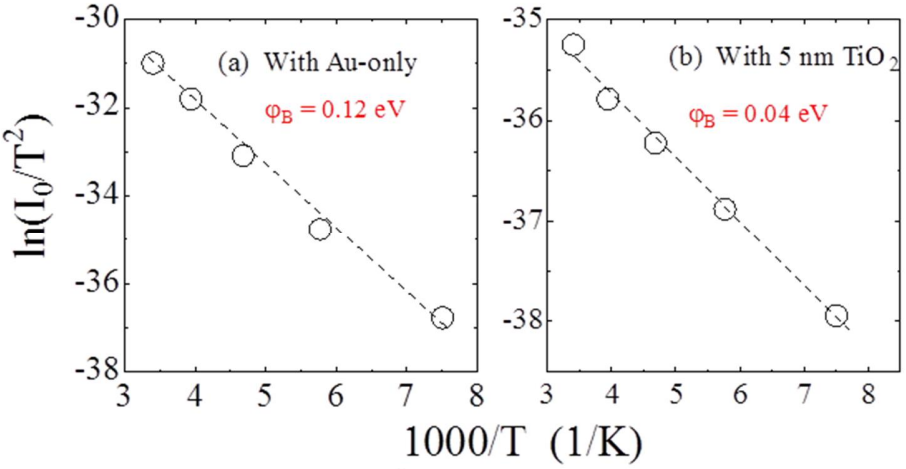

Fig.7.3.4 Relationship between $\ln(I_0/T^2)$ and 1/T.(a) With Au-Only and (b) with 5 nm TiO_2 layer.

Fig.7.3.5 shows the energy level diagrams of different materials used in the device fabrication, TiO_2 and pentacene. At the Au/pentacene interface, there is relatively large hole injection barrier of 0.8 -1 eV. The highest molecular orbitalôs (HOMO) of Au, TiO_2 and pentacene lies at 5.1 eV [19, 28] , 7.4 eV[18-19] and 5. 0 eV [9] respectively. The HOMO of TiO_2 is deeper than the Au and pentacene. Therefore the highest occupied molecular orbital (HOMO) of pentacene aligned with the valence band of TiO_2, resulting in no barrier for injection of holes into the pentacene. Therefore the barrier height is reduced and the device performance is highly improved after inserting a suitable layer of transition metal oxides between the Au electrode and pentacene layer.

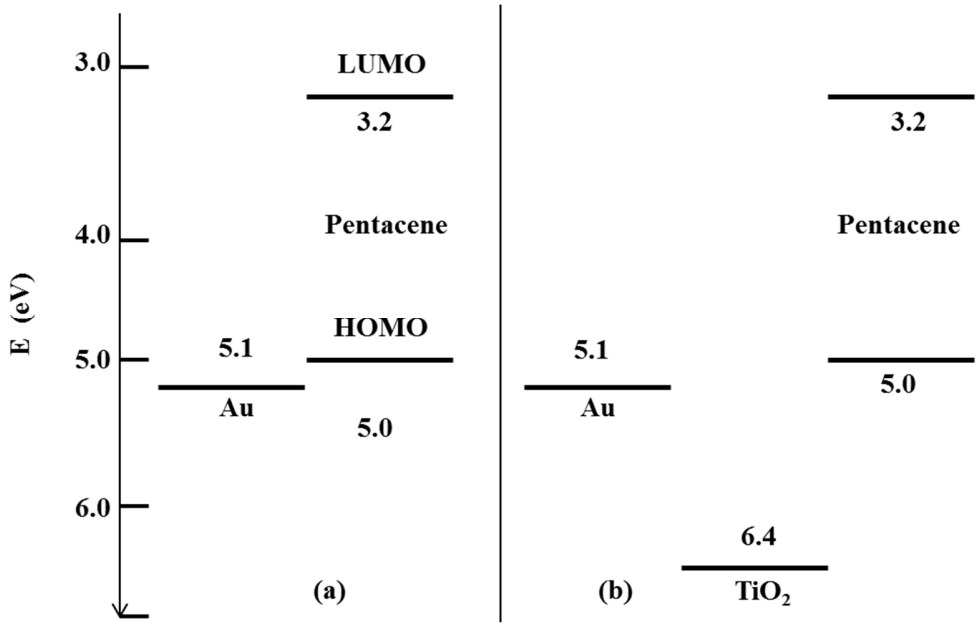

Fig.7.3.5 Energy level diagrams for Au, TiO_2 and pentacene.

Fig.7.3.6 (a) and (b) shows the AFM micrograph of only pentacene layer and with TiO_2 layer, respectively. The pentacene films show typical morphology with large sized dendrites. The root mean square (rms) roughness for both devices with out and with 5 nm TiO_2 is 7.45 nm and 7.05

nm, respectively. It is observed that the surface of pentacene becomes smoother after inserting 5 nm TiO_2 layer. This is also one of the reasons for lowering the barrier height and increasing the charge injection, and then improving device performance. Thus we can conclude that by inserting 5 nm TiO_2 layer between the Au electrodes and pentacene layer play an important role to increase the device performance and mobility.

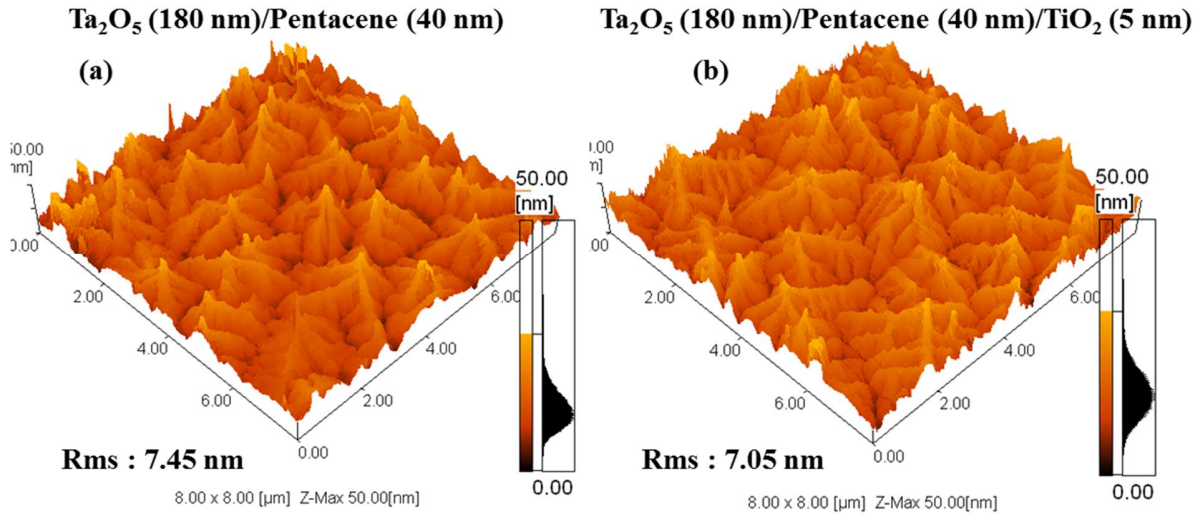

Fig.7.3.6 AFM images of pentacene films (a) with pentacene only (b) with 5 nm TiO_2 layer.

7.4 Conclusion

In Conclusion, we have investigated a Top contact pentacene based OTFTs with bilayer TiO_2/Au electrodes. On comparing the OTFTs with only Au electrode, the performance of the device with bilayer TiO_2/Au electrode is significantly improved. The field-effect mobility increases from (0.37 cm^2 $V^{-1}s^{-1}$) to (0.63 cm^2 $V^{-1}s^{-1}$) and threshold voltage is also decreased. From temperature dependence characteristics the barrier height between the metal and organic layer is evaluated .The barrier height is decreased from 0.12 eV to 0.04 eV in the device with

TiO_2/Au electrodes. The lowered barrier height is due to the smoothed surface of pentacene after inserting TiO_2 layer, which is confirmed by the surface morphology of pentacene. The main parameter for the improvement in the performance of the organic thin film transistor is the decreased barrier height and smoothed surface of pentacene after inserting TiO_2 layer between the Au electrodes and organic semiconductor layer. Therefore, using a transition metal oxide as the hole injection layer is an effective way to improve the characteristics of OTFTs, making the device suitable for commercial applications.

7.5 References

[1] Z. Bao: Adv. Mater. **12**, 227, 2000.

[2] C. D. Dimitrakopoulos and P. R. L. Malenfant: Adv. Mater. **14**, 99, 2002.

[3] S. Liu, Q. Shen, Y. Cao, L. Gan, Z. Wang, M. L. Steigerwald and X. Guo: Coord. Chem. Rev. **254**, 1101, 2010.

[4] H. S. Seo, Y. S. Jang, Y. Zhang, P. S. Abthagir and J. H. Choi: Org. Electron. **9,** 432, 2008.

[5] D. Braga and G. Horowitz: Adv. Mater. **21**, 1473, 2009.

[6] A. L. Deman, M. Erouel, D. Lallemand, M. P. Goutorbe, P. Lang and J. Tardy: J. Non-Cryst. Solids **354**, 1598, 2008.

[7] J. H. Park, C. H. Kang, Y. J. Kim, Y. S. Lee and J. S. Choi: Mater. Sci. Eng. **C 24**, 27, 2004.

[8] Y. Bai, X. Liu, L. Chen, K. Haq, M. A. Khan, W. Q. Zhu, X. Y. Jiang and Z. L. Zhang: Microelectron. J. **38**, 1185, 2007.

[9] Q. J. Sun, Z. Xu, S. L. Zhao, F. J. Zhang, L. Y. Gao and Y. S. Wang: Synth. Met.**160**, 2239, 2010.

[10] S. D. Wang, T. Minari, T. Miyadera, K. Tsukagoshi and Y. Aoyagi: Appl. Phys. Lett. **91**, 203508, 2007.

[11] T. Umeda and S. Tokito: Appl. Phys. Lett. **92**, 013301, 2008.

[12] P. Jeon, K. Han, H. Lee, H. S. Kim, K. Jeong, K. Cho, S. W. Cho and Y. Yi: Synthetic Met. **159**, 2502, 2009.

[13] D. W. Zhao, P. Liu, X. W. Sun, S. T. Tan, L. Ke and A. K. K. Kyaw: Appl. Phys. Lett. **95,** 153304, 2009.

[14] S. Tokito, K. Noda and Y. Taga: J. Phys. D **29**, 2750, 1996.

[15] X. W. Zhang, X. Y. Jiang, M. A. Khan, J. Cao, J. W. Ma, L. Zhang, J. Li, K. U. Haq, W. Q. Zhu and Z. L. Zhang: Solid State Communication. **149**, 652, 2009.

[16] A. Enesca, L. Andronic, A. Duta and S. Manolache: Romanian Journal of Information Sci. Tech. **10**, 269, 2007.

[17] Z. Yang and R. Wu: Physical Rev. B. **61**, 14066, 2000.

[18] C. Y. Kuo, W. C. Tang, C. Gau, T. F. Guo and D. Z. Jeng: Appl. Phys. Lett. **93**, 033307, 2008.

[19] L. Shen, G. Zhu, W. Guo, C. Tao, X. Zhang, C. Liu, W. Chen, S. Ruan and Z. Zhong: Appl. Phys. Lett. **92**, 073307, 2008.

[20] H. Al-Dmour and D. M. Taylor: Appl. Phys. Lett. **94**, 223309, 2009.

[21] C. Y. Kwong, W. C. H. Choy, A. B. D. jurisic, P. C. Chui, K. W. Cheng and W. K. Chan: Nanotech. **15**, 1156, 2004.

[22] S. M. Mok, F. Yan and H. L. W. Chan: Appl. Phys. Lett. **93**, 023310, 2008.

[23] Q. Wei, K. Hirota, K. Tajima and K. Hashimoto: Chem. Mater. **18**, 5080, 2006.

[24] T. W. Zeng, Y. Y. Lin, H. H. Lo, C. W. Chen, C. H. Chen, S. C. Liou, H. Y. Huang and W. F. Su: Nanotechnology **17**, 5387, 2006.

[25] Y. Lou, Z. Wang, S. Naka and H. Okada: Appl. Phys. Lett. **99**, 033305, 2011.

[26] S. Naka, M. Tamekawa, T. Terashita, H. Okada, H. Anada and H. Onnagawa: Synth. Met. **91**, 129, 1997.

[27] I.D. Parker: J. Appl. Phys. **75**, 1656, 1994.

[28] M. N. Shan, S. S. Wang, Z. Q. Bian, J. P. Liu and Y. L. Zhao: Solar Energy Materials & Solar Cells **93**, 1613, 2009.

Chapter 8

Enhanced Carrier Injection in Pentacene Thin-Film Transistors by Inserting a MoO3-Doped Pentacene Layer

We report on the enhanced carrier injection in pentacene thin-film transistors with a thin MoO_3-doped pentacene layer between pentacene semiconductor and the source-drain electrodes. Device performance including drain current, field effect mobility, and threshed voltage are improved by employing a MoO_3-doped pentacene thin layer. The barrier height at the Au/pentacene interface is lowered from 0.12 to 0.05 eV after inserting a MoO_3-doped pentacene thin layer between them. The reduced barrier height is attributed to the formation of a good contact between MoO_3-doped pentacene and Au owing to smoothed surface morphology of pentacene and suitable band bending by MoO_3 doping.

8.1 Introduction

The performance of organic thin-film transistors (OTFTs) has improved significantly in the past several years, and it now appears that there are potential applications in low-cost large-area organic electronics. Recently, some studies have demonstrated that numerous organic materials exhibit carrier mobility comparable to hydrogenated amorphous silicon (a-Si:H) [1-3]. Therein, pentacene is one of the most thoroughly studied p-type materials due to its high mobility. The organic semiconductor, which determines the charge carrier transport as well as the charge carrier injection, is the core element of an OTFT. Both the carrier transport and the carrier injection affect the device performance. It has been shown by Chu et al.[4] that the contact between the source-drain electrodes and the organic semiconductor can be improved by using

carrier injection layers such as molybdenum oxide (MoO_x), vanadium oxide (VO_x), or tungsten oxide (WO_x). Kumaki et al.[5] also reported that the contact resistance in bottom-contact OTFTs can be reduced by using a MoO_x carrier injection layer instead of conventional adhesive layers such as Cr or Ti.

Electrical doping in organic materials is a powerful technology for resolving the problems of low conductivity and high charge injection barriers in organic light-emitting devices (OLEDs),[6ï 8] organic photovoltaic cells (OPVs), and OTFTs.[9, 10] Recently, molybdenum oxide (MoO_3) was mostly used in OLEDs and OTFTs as a buffer layer for efficient carrier injection,[11,12] in tandem OPVs as an interconnecting layer,[13,14] and in various materials as a dopant.[15ï 17] Particularly, the p-doping of pentacene by MoO_3 incorporation has been confirmed by ultraviolet photoelectron spectroscopy and scanning tunneling microscopy studies [18]. In this work, we report the improved performance, especially the device mobility, of a typical top-contact pentacene OTFT by inserting a MoO_3-doped pentacene layer between the pure pentacene layer and the source-drain (S-D) electrodes. We investigated the carrier injection behavior from the S-D electrodes to the pentacene layer through the thin MoO_3-doped pentacene layer by evaluating the temperature-dependence of the drain current-voltage characteristics between them. The barrier height, morphology change, and band conditions in MoO_3-doped and non-doped cases are also investigated.

8.2 Experimental Details

A cross section of the pentacene OTFTs is shown in Fig.8.3.1. The radio-frequency sputtered Ta (50 nm) and Ta_2O_5 (180 nm) serves as the common gate electrode and the gate insulator,

respectively. Then, a 30 nm pentacene layer was thermally evaporated as the active channel layer, followed by a 10 nm MoO_3-doped pentacene (1:4 in weight) layer deposited by co-evaporation. Finally, Au (80 nm) was deposited as S-D electrodes by e-beam evaporation. The channel length (250 lm) and channel width (1 mm) are patterned by a metal mask when depositing pentacene and co-deposition layers. For comparison, a referenced OTFT with 40 nm pentacene and an OTFT with 30 nm pentacene with an additional 10 nm MoO_3 as injection layer were also fabricated. The electrical properties of the fabricated OTFTs were characterized using a semiconductor parameter analyzer (HP 4155B) connected to a probe station. The drain current versus drain voltage (I_D-V_D) curves with varying temperature at a fixed gate voltage of 0V were measured for investigation of carrier transport properties by loading the fabricated devices into a cryostat. The temperature was varied from 293 to 133K by flowing liquid nitrogen into the sample holder in the vacuum chamber.

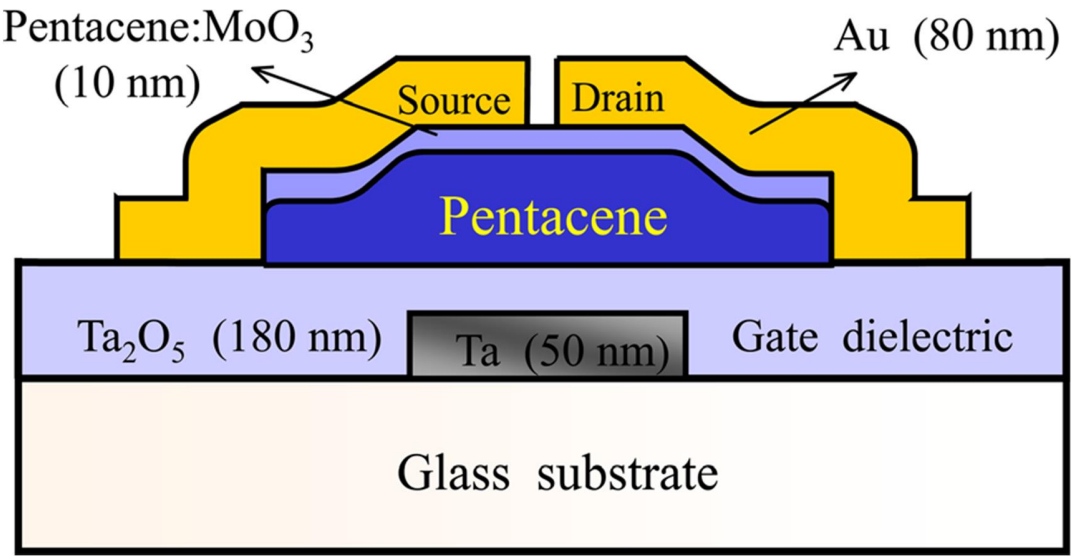

Fig.8.3.1 Device structure of MoO_3-doped pentacene OTFT under investigation.

8.3 Results and Discussion

Figs.8.3.1 (a)ï (c) show the output characteristics of the reference device, an OTFT with 10 nm MoO_3, and an OTFT with 10 nm MoO_3-doped pentacene, respectively. These devices exhibited typical p-channel characteristics. The drain current shows a linear increase with drain voltage, which indicates a good Ohmic contact at the S-D electrodes/organic interfaces in the three devices. By inserting a 10 nm MoO_3 between the pentacene and S-D electrodes, the drain current slightly increased compared with the reference device at a fixed gate voltage. It has been demonstrated that MoO_3 can be used as an injection layer to reduce the contact resistance and injection barrier height between S-D electrodes and the organic layer [19]. Notably, the drain current is largely enhanced when a 10 nm MoO_3-doped pentacene layer was a) inserted between the pure pentacene and S-D electrodes.

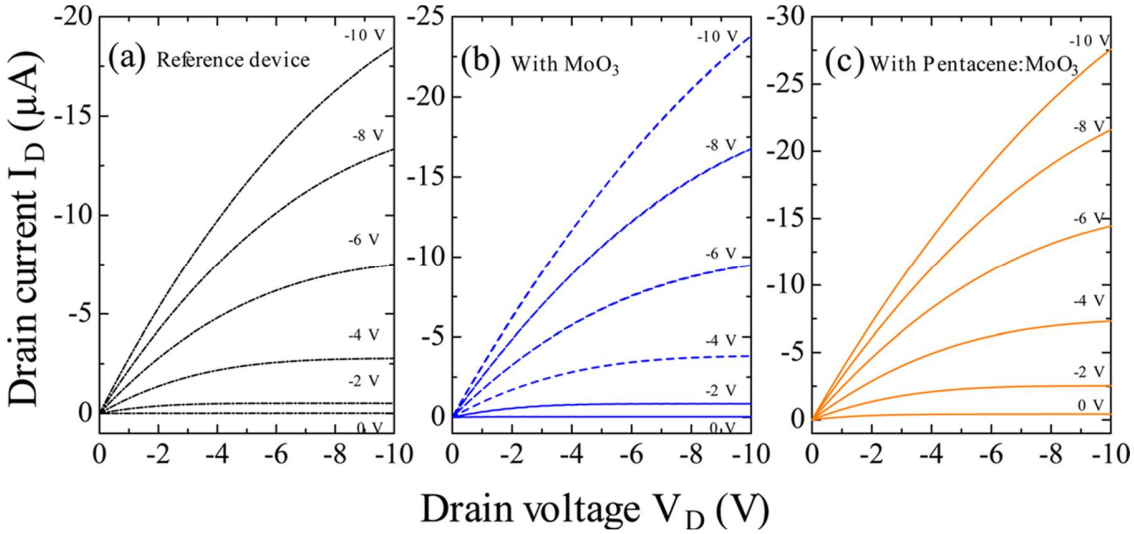

Fig.8.3.1 Drain current vs drain voltage characteristics of pentacene OTFTs. (a) without injection layer; (b)with 10 nm MoO_3 injection layer; and (c) with 10 nm MoO_3-doped pentacene injection layer.

Fig.8.3.2 displays the transfer characteristics in the three OTFTs. All the key parameters, the field effect mobility (μ), on/off ratio, and threshold voltage (V_T) are extracted from the device transfer characteristics. There exists no large difference between the on/off ratio of the three devices. In the reference device, μ and V_T are calculated to be 0.45 cm^2 $V^{-1}s^{-1}$ and 0.9 V, respectively. In the device with 10 nm MoO_3 as injection layer, μ increases to 0.53 $cm^2 V^{-1}s^{-1}$ and V_T is reduced to -1.1 V. After using a 10 nm MoO_3-doped pentacene as injection layer, μ increases to 0.64 $cm^2 V^{-1}s^{-1}$ and V_T is reduced to -3.4 V, demonstrating an obvious improvement in the device performance.

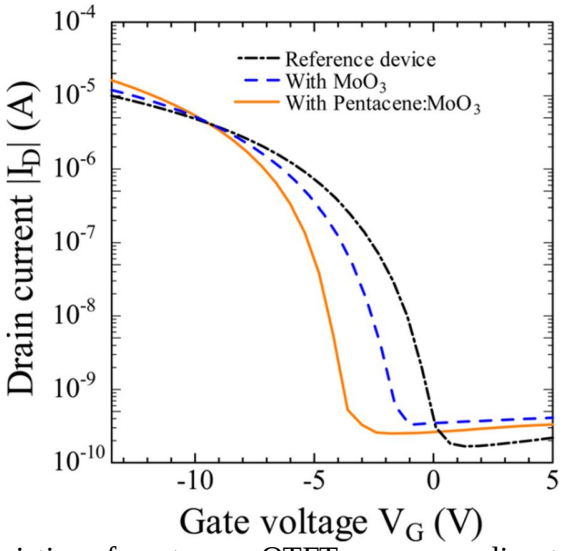

Fig.8.3.2 Transfer characteristics of pentacene OTFTs corresponding to without injection layer, with 10 nm MoO_3 injection layer, and with 10 nm MoO_3-doped pentacene injection layer at VG.-4V.

The performance of organic electronic devices is always strongly affected by the morphology of the organic active layers [20ï 22]. For OTFTs the smoothed organic films with appropriate molecular packing is highly desired to enhance the carrier injection and charge mobility.

However, the organic films associated with OTFTs, such as pentacene, typically show the surface morphology of terraced mounds with high density of molecular steps, which drastically increases the surface roughness [23ï 25]. In the present work, the root mean-square (rms) roughness of MoO_3-doped pentacene films decreased to 3.68 nm compared with 4.55 nm in pure pentacene films (not shown here). It is assumed that doping with MoO_3 slightly reduces the surface roughness of pentacene, which is helpful for generation of a better contact with the electrodes, resulting in lowered barrier height.

On the other hand, the interfacial conditions, including band bending between S-D electrodes and the organic semiconductor also play an important role in carrier injection. It has been shown that the contact between the S-D electrodes and the organic semiconductor can be improved by using a MoO_3 injection layer in top-contact OTFTs [4,5]. In the present work, we further investigate the carrier injection properties by evaluating the temperature dependence of the I_D-V_D curves with varying temperature. Fig. 8.3.3 (a) and (b) show the temperature dependence of the I_D-V_D curves in OTFTs with and without MoO_3-doped pentacene layer, respectively, at a fixed gate voltage of 0 V. As illustrated in Fig. 4, the drain current in the device with 10 nm MoO_3-doped pentacene is up to one order of magnitude higher than that in the device without MoO_3-doped pentacene layer. This is consistent with the performance of the transistor devices as demonstrated in Fig.8.3.1. Particularly, the improvement of drain current is even obvious in the lower drain voltage region. Notably, the I_D-V_D characteristics show strong temperature dependence in both devices. Such temperature-dependent behavior is usually associated with a Schottky thermal emission process for carrier injection at metal/organic interfaces, which is discussed in detail elsewhere [26ï 29]. By plotting the relationship lnI *vs* $V^{1/2}$ and extrapolating

straight lines to the ordinal point, the current at zero voltage I_0 under different temperatures are determined. Using the determined I_0 values, the relationship between lnI_0/T^2 vs $1/T$ is plotted, as shown in Figs. 8.3.3 (c) and (d). The slope of the extrapolated lines gives a barrier height of 0.12 eV at the Au/pentacene interface and 0.05 eV at the Au/MoO_3-doped pentacene interface. Obviously, the hole barrier height is lowered after inserting a thin MoO_3-doped pentacene layer between the pentacene layer and the Au electrode.

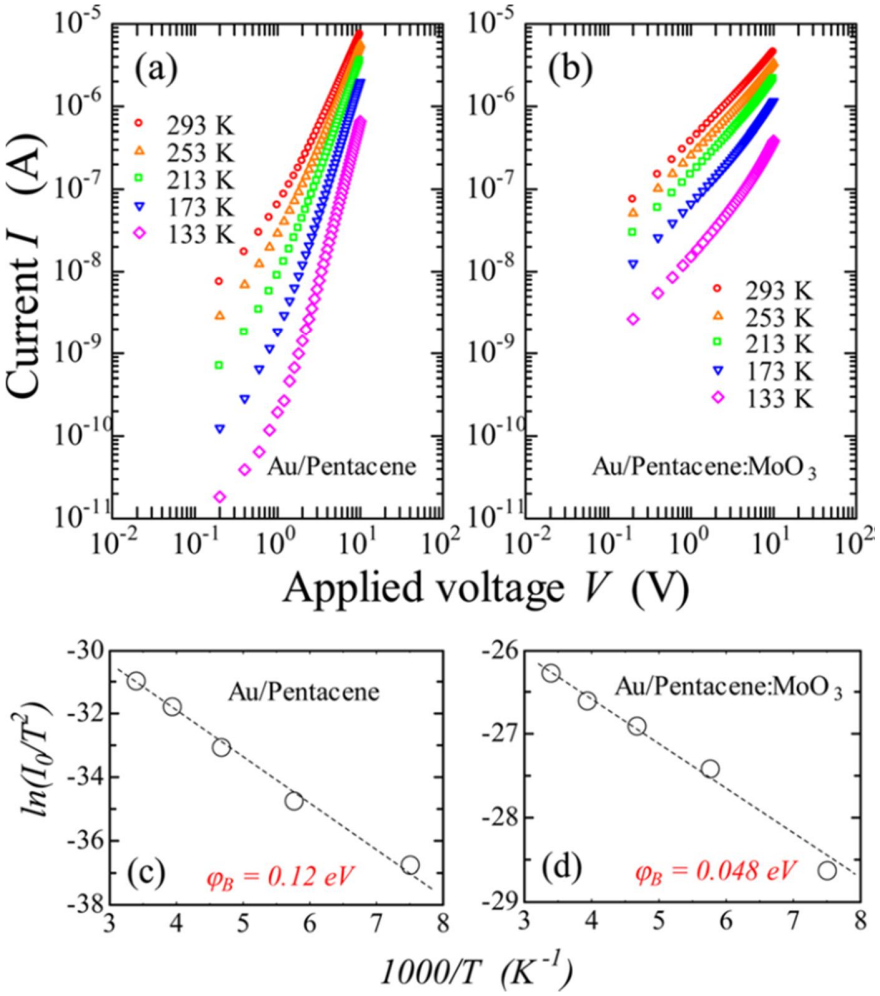

Fig. 8.3.3 Temperature dependence of the I_D-V_D characteristics at a fixed gate voltage of 0V in the OTFTs. (a) without and (b) with 10 nmMoO_3-doped pentacene layer. (c) and (d) are the corresponding relationship between $ln(I_0/T^2)$ and $1/T$.

Fig.8.3.4 shows the energy level diagram of materials under investigation. In the reference device without any injection layer between the pentacene and S-D electrodes, Au directly contacts with pentacene, resulting in a large barrier for holes. By inserting a thin MoO_3 layer between them, the contact resistance is reduced and the contact conditions are improved owing to the high conduction band value of MoO_3. For MoO_3-doped pentacene, the offset between the highest occupied molecular orbital (HOMO) and Fermi energy (EF) of pentacene decreases with MoO_3 doping, and the ionization energy of pentacene does not change upon MoO_3 doping because no chemistry occurs between MoO_3 and pentacene [18] Therefore, by inserting a thin MoO_3-doped pentacene layer between the pentacene and Au, a strong energy band bending as shown in Fig.8.3.4 (c) occurs when Au contacts with MoO_3- doped pentacene owing to good aligning of the MoO_3 conduction band with the HOMO of pentacene. The band bending makes it possible for the formation of a good contact between pentacene and the S-D electrodes, which can effectively lower the barrier height for hole injections. In addition, it has been proved that transition metal oxides with very high conduction band energy can form charge transfer (CT) complexes with organic semiconductors [30, 31]. For example, CT complexes are easily formed when doping MoO_3 into N, N0-diphenyl-N, N0- bis-(1-naphthyl)-1-10-biphenyl-4,40-diamine (a-NPD) [31]. It is assumed that CT complexes are also formed in MoO_3-doped pentacene, which contribute to an increase of charge carrier density in pentacene, resulting in enhanced conductivity of pentacene and improved device performance.

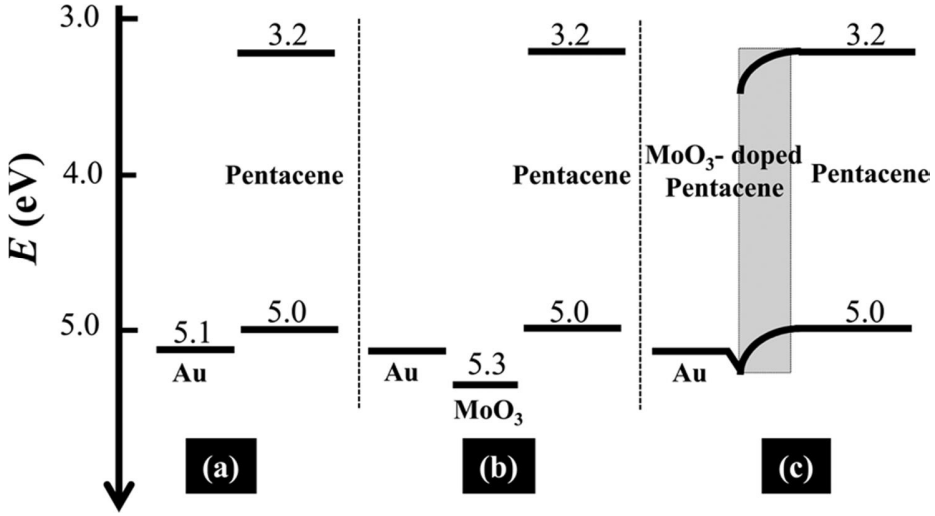

Fig. 8.3.4 A schematic energy level of the materials under investigation for (a)without injection layer; (b) with 10 nm MoO_3 injection layer; and (c) with10 nm MoO_3-doped pentacene injection layer.

8.4 Conclusion

In summary, we have demonstrated a pentacene thin film transistor with a thin MoO_3-doped pentacene layer used as injection layer. Enhanced hole injection and improved device performance are observed compared with a reference device using pure MoO_3 as injection layer. The hole barrier height was lowered to 0.05 eV as determined by evaluating the temperature-dependence of the I_D-V_D characteristics. With suitable MoO3 doping into pentacene, the surface morphology of pentacene was smoothed by atom force microscopy (AFM) observation,32 band bending occurred owing to good aligning of MoO_3 conduction band with the HOMO of pentacene, resulting in the formation of a good contact between MoO_3-doped pentacene and Au.

8.5 References

[1] S. F. Nelson, Y. Y. Lin, D. J. Gundlach and T. N. Jackson: Appl. Phys. Lett. **72**, 1854, 1998.

[2] Y. N. Li, Y. L. Wu, S. Gardner, and B. S. Ong, :Adv. Mater. (Weinheim, Ger.) **17**, 849, 2005.

[3] A. L. Briseno, M. Roberts, M. M. Ling, H. Moon, E. J. Nemanick and Z. N. Bao: J. Am. Chem. Soc. **128**, 3880, 2006.

[4] C. W. Chu, S. H. Li, C. W. Chen, V. Shrotriya and Y. Yang: Appl. Phys. Lett. **87**, 193508 2005.

[5] D. Kumaki, T. Umeda, and S. Tokito: Appl. Phys. Lett. **92**, 013301, 2005.

[6] S. Reineke, F. Lindner, G. Schwartz, N. Seidler, K. Walzer, B. Lussem, and K. Leo: Nature (London) **459**, 234, 2009.

[7] S. Hamwi, T. Riedl, and W. Kowalsky: Appl. Phys. Lett. **99**, 053301, 2011.

[8] J. Qiu, Z. B. Wang, M. G. Helander, and Z. H. Lu: Appl. Phys. Lett. **99**, 153305, 2011.

[9] C. K. Chan, W. Zhao, A. Kahn, and I. G. Hill: Appl. Phys. Lett. **94**, 203306, 2009.

[10] S. P. Tiwari, W. J. Potscavage, Jr., T. Sajoto, S. Barlow, S. R. Marder and B. Kippelen: Org. Electron. **11**, 860, 2010.

[11] J. Meyer, S. Hamwi, T. Bu¨low, H. H. Johannes, T. Riedl and W. Kowalsky: Appl. Phys. Lett. **91**, 113506, 2007.

[12] C.-W. Chu, S.-H.Li, C.-W. Chen, V. Shrotriya and Y. Yang: Appl. Phys. Lett. **87**, 193508, 2005.

[13] A. G. F. Janssen, T. Riedl, S. Hamwi, H. H. Johannes and W. Kowalsky: Appl. Phys. Lett. **91**, 073519, 2007.

[14] F.-C. Chen and C.-H. Lin: J. Phys. D: Appl. Phys. **43,** 025104, 2010.

[15] W.-J. Shin, J.-Y.Lee, J. C. Kim, T.-H.Yoon, T.-S. Kim and O.K. Song: Org. Electron. **9**, 333, 2008.

[16] S. Hamwi, J. Meyer, T. Winkler, T. Riedl and W. Kowalsky: Appl. Phys. Lett. **94**, 253307, 2009.

[17] M. Kroger, S. Hamwi, J. Meyer, T. Riedl, W. Kowalsky and A. Kahn: Org. Electron. **10**, 932, 2009.

[18] S. D. Ha, J. Meyer and A. Kahn: Phys. Rev. B **82** 155434, 2010.

[19] D. Kumaki, T. Umeda and S. Tokito: Appl. Phys. Lett. **92**, 013302, 2008.

[20] Y. Kim, M. Shin, H. Kim, Y. Ha and C. S. Ha:J. Phys. D. Appl. Phys. **41**, 225101, 2008.

[21] Z. Wang, Y. Lou, S. Naka and H. Okada: Appl. Phys. Lett. **98**, 063302, 2011.

[22] Z. Wang, Y. Lou, S. Naka and H. Okada: ACS Appl. Mater. Interface **3**, 2496 2011.

[23] Y. Lou, Z. Wang, S. Naka and H. Okada: Appl. Phys. Lett. **99**, 033305, 2011.

[24] H. Klauk: Chem. Soc. Rev. **39,** 2643, 2010.

[25] A. A. Virkar, S. Mannsfeld, Z. N. Bao and N. Stingelin: Adv. Mater. (Weinheim, Ger.) **22**, 3857, 2010.

[26] D. Knipp, R. A. Street and A. R. Volkel:Appl. Phys. Lett. **82**, 3907, 2003.

[27] F. Dinelli, M. Murgia, P. Levy, M. Cavallini, F. Biscarini and D. M. deLeeuw: Phys. Rev. Lett.**92**, 116802, 2004.

[28] H. L. Cheng, Y. S. Mai, W. Y. Chou, L. R. Chang and X. W. Liang: Adv. Funct. Mater. (Weinheim, Ger.) **17**, 3639, 2007.

[29] S. Wang, T. Minari, T. Miyadera, Y. Aoyagi, and K. Tsukagoshi; Appl. Phys. Lett. **93**, 043311, 2008.

[30] C.-C. Chang, M.-T. Hsieh, J. F. Chen, S.-W. Hwang and C. H. Chen: Appl. Phys. Lett. **89**, 253504, 2006.

[31] F. Wang, X. Qiao, T. Xiong and D. Ma: Org. Electron. **9**, 985, 2008.

Chapter 9

Summary

Organic thin-film transistors (OTFTs) have attracted increasing interest for their potential advantages, such as, low cost, lightweight and possible fabricating on flexible substrate, as well as large-area feasibility. For constructing a high performance top-contact OTFT, it is very important to understand the influence of interfaces, which play a crucial role in the overall performance of the device. Mainly there are two kinds of interfaces in the OTFT. First is in between the semiconductor and the gate dielectric, where the conducting channel forms. The second one is in between the source/drain (S/D) electrodes and the semiconductor layer where charge carriers are injected.

The interface between the organic and metal electrode was studied. Organic and metal interfaces mostly limit the performance of the device and field effect mobility is also decreased. In earlier reports it has been shown that the diffusion between the metal electrode and pentacene reduce the hole injection carrier at the interface which causes the increase in barrier height and contact resistance which effect the performance of the OTFTs. It is shown that the contact between the S/D electrodes and the organic semiconductor can be improved by inserting transition metal oxide layer as carrier injection layers. Because of good electronic properties, transition metal oxides such as molybdenum oxide (MoO_3), tungsten oxide (WO_3) and vanadium oxide (V_2O_5), and other oxides such as germanium oxide (GeO), titanium oxide (TiO_2) offer a unique opportunity to control the work function, and hence increase the charge-injection properties. Therefore, by modifying the organic/electrode interface, the S/D electrodes do not

directly contact with pentacene layer and hence significantly reduces the contact resistance, barrier height and provides protection from diffusion and other chemical reactions, which increase device performance.

We investigated that the charge injection and field effect mobility is enhanced by inserting a thin (5 nm) MoO_3, GeO, WO_3 and TiO_2 interlayer between the Au electrode and pentacene layer in a top contact pentacene based organic thin-film transistor (OTFTs). In comparison with the pentacene-based OTFT with only-Au electrode, the device performance with bilayer electrode has been considerably improved. The device performance including field effect mobility, threshold voltage, and On/Off ratio of all the device after modification was highly improved, and the highest mobility of 0.96 $cm^2V^{-1}s^{-1}$, threshold voltage of -4 V, and highest on/off ratio of 5.2×10^4 were achieved in the device with 5 nm GeO. I further investigated the temperature dependence of I_D–V_D characteristics which showed strong temperature dependence in all the devices.

We further studied the obvious temperature dependence of I_D-V_D curves in all devices. We observed that the charge injection characteristics can be fitted by the Schottky emission mechanism. We plottted the relationship between $ln(I)$ vs $V^{1/2}$ and extrapolating straight lines to the ordinal point, the current at zero voltage I_0 is determined. By using the values of I_0, the relationship between $ln(I_0/T^2)$ vs $1/T$ is plotted and from the resulting slope of extrapolated lines. While in case of bilayer MoO_3/Au shows 0.03 eV, WO_3/Au shows 0.05 eV, TiO_2/Au showed 0.04 eV and with only Au electrodes barrier height of 0.12 eV is achieved. The lowest barrier heights of 0.01 eV could be achieved in case of bilayer GeO/Au electrodes. It is assumed that the

barrier height was dramatically reduced by inserting thin oxide layer between the Au and pentacene layer.

Similarly, from surface morphology of pentacene, the root mean square roughness is also decreased after inserting metal oxide layer. The main factor for the improvement in the performance of the OTFTs with bilayer electrodes was explained in terms of the reduction in barrier height and smoothed surface roughness of active layer. Therefore, the combination of a thin oxide layer with Au as a bi-layer electrode is an effective way to improve the characteristics of OTFTs, which makes the device suitable for commercial applications.

Finally, I further reported the enhanced carrier injection in pentacene OTFTs with a thin MoO_3-doped pentacene layer between pentacene semiconductor and the S/D electrodes. Device performance including drain current, field effect mobility, and threshed voltage are improved by employing a MoO_3-doped pentacene thin layer. The barrier height at the Au/pentacene interface is lowered from 0.12 to 0.05 eV after inserting a MoO_3-doped pentacene thin layer between them.

In summary, I have studied bi-layer S/D contact of metal oxide/ electrode structure by applying OTFT. Obtained barrier height is as small as 0.01 eV for GeO/ Au structure, which value is lower than that of conventional MoO_3/Au structure of 0.03 eV. Therefore, GeO/Au bi-layer electrode structure is promising for other kinds of electrodes structure. In addition, effectiveness of doped pentacene with MoO_3 is designated. These device structures are promising for OTFT application and exhibited best performance reported to date.

Chapter 10

Publications and conferences

10.1 International Published Papers

1.Z. Wang, M. W. Alam, Y. Lou, S. Naka, H. Okada, ñEnhanced Carrier Injection in Pentacene Based Thin Film Transistor by Inserting a Thin Pentacene-MoO_3 Co-deposition Layerò, Appl. Phys. Lett. **100**, 043302 (2012).

2.M. W. Alam, Z.Wang, S. Naka and H. Okada: "Top Contact Pentacene Based Organic Thin Film Transistor with Bi-layer TiO_2/Au Electrodes", J. Photopolymer Sci. & Tech. **25(5)**, pp.659-664 (2012).

3.M. W. Alam, Z.Wang, S. Naka and H. Okada: "Mobility enhancement of top contact pentacene based organic thin film transistor with bi-layer GeO/Au electrodes", Appl. Phys. Lett. **102**, 061105 (2013).

4.M. W. Alam, Z.Wang, S. Naka and H. Okada: "Performance Enhancement of Top-Contact Pentacene-Based Organic Thin-Film Transistors with Bilayer WO_3/Au Electrodes", Jpn. J. Appl. Phys. **52** (2013) 03BB08.

5. M. W. Alam, Z.Wang, S. Naka and H. Okada: "Temperature Dependence of Barrier Height and Performance Enhancement of Pentacene Based Organic Thin Film Transistor with Bi-Layer MoO_3/Au Electrodes" Current Nano Science under review.

10.2 International Conferences

1.M. W. Alam, Z. Wang, S. Naka, H. Okada, ñPentacene based thin film transistor with bilayer MoO_3/Au electrodeò, The 18th International Display Workshop (IDWô11), OLEDp-4 (2011).
2.M.W.Alam, Z.Wang, S. Naka and H. Okada: "Improved performance of Top Contact Organic Thin film Transistors With bilayer WO_3/Au Electrodes", The 19th Int'l Workshop on Active-Matrix Flat panel Displays and Devices, TFTpP-28 (2012).
3.M. W. Alam, Z. Wang, S. Naka and H. Okada: "Pentacene Based Organic Thin Film

Transistor with Bi-layer TiO_2/Au Electrodes", 29th International Conference of Photopolymer Science and Technology (ICPST-29), A-44 (2012).

4.M. W. Alam, Z. Wang, S. Naka and H. Okada: "Bi-layer GeO_2/Au Au Electrodes For Top Contact Pentacene Based Organic Thin Film Transistor", The 2012 International Conference on Flexible and Printed Electronics, S13-P3 (2012).

10.3 National Conferences

1.M. W. Alam, Z. Wang, S. Naka, H. Okada: ñTop Contact Pentacene Based Organic Thin Film Transistor with Bi-layer Metal Oxide/Au Electrodesò, 平成24年春季応用物 理学関係連合講演会，15p-GP11-14(2012).

2.王、M. W. Alam、中、岡田：ñ酸化物半導体ドープしたペンタセン薄膜トランジス タò、平成24年春季応用物 理学関係連合講演会，15p-GP11-10 (2012).

3.M. W. Alam, 王，中，岡田：" Improved Performance of Top Contact Pentacene Based Organic Thin Film Transistor With bilayer Metal Oxide/Au Electrodes" 平成24年秋季応用物理学会学術講演会，13p-PB2-1 (2012).

4.M. W.Alam, 王，中岡田：" Different Back-exposure Condition for Self-alignment Organic Thin-Film Transistor "，2013年第60回応用物理学会春季学術講演会,