BRIEF PAPER Effects of oscillator phase noise on frequency delta sigma modulators with a high oversampling ratio for sensor applications

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SUMMARY Frequency delta sigma modulation (FDSM) is a unique analog to digital conversion technique featuring large dynamic range with wide frequency band width. It can be used for high performance digitaloutput sensors, if the oscillator in the FDSM is replaced by a variable frequency oscillator whose frequency depends on a certain external physical quantity. One of the most important parameters governing the performance of these sensors is a phase noise of the oscillator. The phase noise is an essential error source in the FDSM, and it is quite important for this type of sensors because they use a high frequency oscillator and an extremely large oversampling ratio. In this paper, we will discuss the quantitative effects of the phase noise on the FDSM output on the basis of a simple model. The model was validated with experiments for three types of oscillators.

key words: delta sigma modulation, frequency delta sigma modulation, phase noise, microwave oscillator

1. Introduction

Frequency delta-sigma modulation is a unique analog-todigital conversion technique based on a voltage controlled oscillator (VCO) [1]–[11]. This technique requires no feedback digital-to-analog converter nor integrator restricting the operation frequency of the conventional delta-sigma modulators (DSMs). It features very high operating frequencies together with the advantages of conventional DSMs, such as, a wide dynamic range and high signal-to-noise ratio (SNR) without using high-precision analog components [12]–[15]. One of the main applications of the FDSM is to use it as a multiple-valued quantizer in higher order DSMs.

The FDSM can also be used for digital output sensors when the VCO is replaced by the oscillator whose oscillation frequency depends on an external physical parameter. The oversampling ratio (OSR) of such sensors should be very large to obtain high SNR, because the FDSM works only as a first order DSM. Moreover, to make use of such large OSRs, the oscillation frequency of the oscillator should be also high, in the microwave to millimeter wave frequency range. We have already proposed and demonstrated such sensors using a high electron mobility transistor (HEMT) and a resonant tunneling diode (RTD) [16]–[20]. However, such high frequency oscillators are often deteriorated by phase noise [21]–[24]. It is, thus, important to know the effects of the phase noise of the oscillator on the high OSR FDSM. Though M. Høvin et al. [1], [25] has mentioned that

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Fig. 1 Block diagram of the frequency delta-sigma modulator.

the phase noise should be first-order noise shaped, details are not yet clear. In this paper, we propose a simple model and a formulation of the effects of the phase noise on the FDSM. This makes it possible to compare the effects of the phase noise with those of the quantization noise directly. Its validity is demonstrated with experimental results.

2. Modeling of the phase noise in FDSM

2.1 Frequency delta-sigma modulation

A simplified block diagram of an FDSM is shown in Fig. 1. It consists of a VCO, a binary quantizer, a register, and an XOR gate. The oscillator outputs a frequency modulation (FM) signal, which can be easily converted to the pulse density modulation (PDM) digital signal using a register and an XOR. The FDSM has a significant advantage that it has no feedback loop nor integrator restricting the operation frequency, in addition to the features of the conventional DSMs.

2.2 Phase noise model

First, to clarify the effects of the phase noise, one must distinguish high frequency white noise and low frequency $f^{-\alpha}$ noise ($\alpha \ge 1$), where f is an offset from the carrier frequency [26]. The former can be modified by the noise shaping, and it has little effects on the output of the FDSM sensors [25]. On the other hand, the latter noise has a significant effects on the output signal. These noises can be regarded as frequency fluctuation, so that it cannot be distinguished from the input signal for the FDSM.

We model the $f^{-\alpha}$ noise as the modulation of the oscillator's frequency by many independent oscillators with an amplitude of a_k [27], [28], which are distributed uniformly in the frequency range with an interval of the frequency f_0 , as shown in Fig. 2. The sinusoidal input signal is assumed and also shown in the figure. The output voltage of the oscillator, V(t), is expressed by

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Fig. 2 A model of phase noise source by uniformly distributed oscillators.

$$V(t) = V_0 \sin\left(2\pi \int_0^t (f_c + f_N(\tau))d\tau\right).$$
 (1)

Here, V_0 , f_c , $f_N(\tau)$ are the output voltage amplitude, carrier frequency, and frequency fluctuation due to the $f^{-\alpha}$ noise, respectively. For simplicity, the signal source is excluded in this equation. The frequency noise is modeled as

$$f_{\rm N}(t) = \sum_{k} a_k \sin(2\pi k f_0 t + \phi_k).$$
 (2)

Here, ϕ_k is a random initial phase of each oscillator. Substituting eq. 2 in eq. 1, we obtain

$$V(t) = V_0 \sin\left(2\pi f_c t - \sum_k \frac{a_k}{kf_0} \cos(2\pi k f_0 t + \phi_k) + \phi_0\right).$$
 (3)

Here,

$$\phi_0 = \sum_k \frac{a_k}{kf_0} \cos(\phi_k) \tag{4}$$

is a total initial phase component. We assume that the noise is so small that first order approximation, $sin(x+\delta) \sim sin x + \delta cos x$, can be used. Then, the output voltage becomes

$$V(t) \sim V_0 \sin(2\pi f_c t + \phi_0) -V_0 \cos(2\pi f_c t + \phi_0) \sum_k \frac{a_k}{k f_0} \cos(2\pi k f_0 t + \phi_k)$$

= $V_0 \sin(2\pi f_c t + \phi_0) -\frac{V_0}{2} \sum_k \frac{a_k}{k f_0} \{\cos(2\pi (f_c + k f_0)t + \phi_0 + \phi_k) + \cos(2\pi (f_c - k f_0)t + \phi_0 - \phi_k)\}.$ (5)

This indicates that the noises with the amplitude of $V_0 a_k/(2kf_0)$ are added at the frequency $f_c \pm kf_0$. Consequently, the phase noise $\mathcal{L}(f)$ can be obtained by dividing the squared noise amplitudes by carrier power and f_0 .

$$\mathcal{L}(f) = \frac{a(f)^2}{4f^2 f_0},\tag{6}$$

where $a(f) = a_k$ for $kf_0 \le f < (k+1)f_0$. When all of the oscillator amplitudes, a_k , are identical, this yields -20 dB/dec dependence for the $\mathcal{L}(f)$.

2.3 Noise in the FDSM output spectrum

The frequency fluctuation by phase noise can not be distinguished from the signal, and it makes the noise floor in the output signal spectrum as implicated in Fig. 2. To clarify the relation between the phase noise and the noise in the FDSM output, we use a simple approximation.

We assume that the sampling frequency is so high that the output of the FDSM can be approximated by a continuous pulse density function PD(t) as

$$PD(t) = \frac{f(t)}{f_{s}/2} = \frac{2f(t)}{f_{s}}.$$
(7)

Here, f(t), f_s are the instantaneous frequency of the oscillator and the sampling frequency, respectively. The output of the FDSM is 1111... for $f(t) = f_s/2$, while it is 0000... for f(t) = 0 or $f(t) = f_s$. This indicates that full-scale input is $f_s/4$ at the center frequency of $f_c = f_s/4$. Therefore, with the full-scale sinusoidal input, the PD(t) is expressed as,

$$PD(t) = \frac{2}{f_{s}} \left[f_{c} + \frac{f_{s}}{4} \sin(2\pi f_{sig}t) + \sum_{k} a_{k} \sin(2\pi k f_{0}t + \phi_{k}) \right].$$
(8)

The 3rd term in the parenthesis indicates that the noise of power density $a_k^2/(2f_0)$ per Hz is added to the FDSM signal at the frequency, $k f_0$. To compare this with the quantization noise, we normalize this noise by the full-scale range, $f_s/4$.

$$p_{\varphi}(f) = \frac{a(f)^2/(2f_0)}{(f_s/4)^2/2} = \frac{16a(f)^2}{f_s^2 f_0} = \frac{64f^2 \mathcal{L}(f)}{f_s^2} \quad (9)$$

This equation relates the phase noise, $\mathcal{L}(f)$, to the noise floor of the FDSM output, $p_{\varphi}(f)$. For identical a_k 's, $\mathcal{L}(f)$ is proportional to f^{-2} , so that, the FDSM noise due to the phase noise is constant.

2.4 Quantization noise

To compare the noise floor due to the phase noise, the quantization noise should also be normalized to the full-scale range. Noise power density of the first order DSM is given by [29]

$$S_{\rm Q}(f) = \frac{2\Delta^2}{3f_{\rm s}}\sin^2\left(\frac{\pi f}{f_{\rm s}}\right) \tag{10}$$

where, the Δ is a quantization step. The quantization noise power density can be obtained by dividing $S_Q(f)$ by fullscale power of 1bit quantizer as

$$p_{\rm Q}(f) = \frac{16}{3f_{\rm s}} \sin^2\left(\frac{\pi f}{f_{\rm s}}\right) \simeq \frac{16\pi^2 f^2}{3f_{\rm s}^3}.$$
 (11)

2.5 Phase noise of the sampling clock

The phase noise of the sampling clock can also be analyzed by the similar model. The pulse density function PD(t)including frequency fluctuation of both the carrier frequency, Δf_c , and the sampling clock, Δf_s , can be expressed as



Fig.3 Comparison of the FDSM noises for three types of oscillators. The figures show the measured phase noise, calculated FDSM noise power, and the measured FDSM noise power, from top to bottom, respectively. Moving averages are also plotted in the top and bottom figures. Left column:resonant tunneling diode oscillator (1.25 GHz) [20], Center column:Keysight 83650L CW Generator (250 MHz), Right column:Crystek CRBSCS-01-250.000 clock source (250 MHz). The measured phase noise of the Crystek clock source is limited by the noise floor of the spectrum analyzer (-117dBc/Hz).

$$PD(t) = 2\frac{f_{c} + \Delta f_{c}}{f_{s} + \Delta f_{s}} \simeq \frac{2}{f_{s}} \left(f_{c} + \Delta f_{c} - \frac{f_{c}}{f_{s}} \Delta f_{s} \right).$$
(12)

This indicates that the effect of Δf_s is smaller than that of the Δf_c by a factor of (f_c/f_s) . Thus, the noise power density due to the phase noise of the sampling clock is expressed as

$$p_{\varphi_{\rm S}}(f) = \frac{64f^2 \mathcal{L}_{\rm s}(f)}{f_{\rm s}^2} \left(\frac{f_{\rm c}}{f_{\rm s}}\right)^2.$$
(13)

This indicates that the lower carrier frequency is advantageous for suppressing the phase noise effects of the sampling clock. However, in general case, higher oscillation frequency leads to larger frequency modulation width, which enhances the sensitivity. Therefore it is advantageous to down-convert high frequency FM signal.

3. Experiments

We have measured the phase noise of various types of oscillators, and calculated the noise properties of the FDSM from these phase noise data. Then, these noises were compared with the outputs of the FDSM employing these oscillators. For this purpose, we fabricated a 10Gb/s-class sampling FDSM circuit on a field programmable gate array (FPGA). We used the FPGA evaluation board, Xilinx ZCU-102. The FDSM circuit comprises a high-frequency sampler, an edge detector, and a digital-filter. A high-frequency transceiver module was used for the sampling circuit, which could be operated at a sampling rate of as high as 16.3 Gb/s. Here, the sampling rate was chosen to be 12.582912 Gb/s, which corresponds to a oversampling ratio of 2¹⁶ for a signal bandwidth of 96 kHz. The details of the FDSM circuit are described in the previous paper [20], [30].

Figure 3 shows examples of the results. The figures show the measured phase noise, calculated FDSM noise power, and the measured FDSM noise power, from top to bottom, respectively. The phase noises were measured using Keysight 8565EC spectrum analyzer. The FDSM noise powers were corrected using the effective noise band width (ENBW), and they were plotted per Hz. Three types of oscillators are shown in the figure. The left column shows the results of the RTD oscillator used for the delta-sigma modulation microphone sensor [20]. It consists of an RTD and a disk-shaped microstrip resonator on FR-4 substrate. It shows relatively high phase noise with a simple -20 dB/dec-like dependence, and it was difficult to measure under 1 kHz. The calculated FDSM noise power is as large as -170 dBFS at high frequency, and increases slightly when decreasing the frequency. This is in good agreement with the experimental result shown in the bottom figure.

The center column shows the results of the Keysight 83650L CW generator. The generator shows much smaller phase noise. It also shows a unique step-like structure at around 40 kHz and small peak at 3 kHz because of the phase locked loop (PLL). In the calculated FDSM noise power, it is shown that the phase noise dominates at frequencies lower than 40 kHz, while the quantization noise dominates higher than this frequency. The calculated noise power also agrees well with the measured value.

The right column shows the results of Crystek CRBSCS-01-250.000 crystal oscillator. This has very small phase noise, and the calculated FDSM noise is also very low. It is shown that the FDSM noise due to the phase noise is much smaller than the quantization noise at frequencies higher than 1 kHz. As shown in the bottom figure, the FDSM noise agrees well with the calculated quantization noise at nearly all frequencies. This indicates that the FDSM noise can be further reduced by increasing the sampling frequency.

It is noted that the phase noise of the sampling clock has no noticeable effect on the FDSM noise floor because of relatively small carrier frequency as discussed in 2.5.

4. Conclusion

Effects of the phase noise on the FDSM is discussed. Simple model of the FDSM noise is proposed to evaluate them quantitatively. The validity of the model is demonstrated with three types of oscillators.

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References

- M. Høvin, T. S. Lande, C. Toumazou, "Delta-Sigma Modulators Using Frequency-Modulated Intermediate Values," IEEE J. Solid-State Circuits 32, pp. 13–22, 1997.
- [2] A. Iwata, N. Sakimura, M. Nagata and T. Morie, "The Architecture of Delta Sigma Analog-to-Digital Converters Using a Voltage-Controlled Oscillator as a Multibit Quantizer," IEEE Trans. Circuits and Systems-II 46, pp. 941–945, 1999.
- [3] K. Maezawa, M. Sakou, W. Matsubara and T. Mizutani, "Resonant tunneling delta-sigma modulator suitable for high-speed operation," Electron. Lett. 42, 20063215, 2006.
- [4] K. Maezawa, M. Sakou, W. Matsubara, T. Mizutani, "Dual-clock MASH delta-sigma modulator employing a frequency modulated interemediate signal," IEICE Electron. Express, Vol. 3, pp. 459-463, 2006.
- [5] M. Z. Straayer, and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous- time ADC with a 5-bit, 950-MS/s VCO-based quantizer," IEEE J. Solid-State Circ. 43, p. 805, 2008.
- [6] Min Park, and M.H. Perrott. "A VCO-based analog-to-digital converter with second-order Sigma-Delta noise shaping." IEEE Int. Symp. Circ. Sys. ISCAS 2009, 3130-3133.
- [7] M. Voelker, S. Pashmineh, J. Hauer, M. Ortmanns, "Current Feedback Linearization Applied to Oscillator Based ADCs," IEEE Trans. Circ. Sys. I, Vol. 61, pp. 3066-3074, 2014.

- [8] K. Lee, Y. Yoon, and N. Sun, "A Scaling-Friendly Low-Power Small-Area ADC With VCO-Based Integrator and Intrinsic Mismatch Shaping Capability," IEEE J. Emerg. Selec. Topics Circ. Sys., Vol. 5, pp. 561-573, 2015.
- [9] X. Xing, P. Zhu, H. Liu, G. Gielen, "Fully-VCO-based 0-2 MASH CT $\Delta \Sigma$ ADC," Electron. Lett., Vol. 54, pp. 1018-1020, 2018.
- [10] S. Li, A. Sanyal, K. Lee, Y. Yoon, X. Tang, Y. Zhong, K. Ragab, and N. Sun, "Advances in Voltage-Controlled-Oscillator-Based ΔΣ ADCs," IEICE Trans. Electron., Vol.E102-C, pp. 509-519, 2019.
- [11] A. Jayaraj, M. Danesh, S. T. Chandrasekaran, A. Sanyal, "Highly Digital Second-Order VCO ADC," IEEE Trans. Circ. Sys. I, vol. 66, no. 7, pp. 2415-2425, 2019.
- [12] Candy, C., (1974), "A Use of Limit Cycle Oscillations to Obtain Robust Analog-to-Digital Converters," IEEE Trans. on Commun., vol. 22, no. 3, pp. 298–305.
- [13] S. R. Norsworthy, R. Schreier, G. C. Temes, *Delta-Sigma Data Converters*, IEEE Press, New York, USA, 1996.
- [14] S. R. Pavan, R. Schreier, G. C. Temes, "Understanding Delta-Sigma Data Converters (2nd Ed.)," Willey & Sons, New Jersey, 2017.
- [15] S. Dosho, "Continuous-Time Delta-Sigma Modulators: Tutorial Overview, Design Guide, and State-of-the-Art Survey," IEICE Trans. Electron., Vol. E95-C, No. 6, pp. 978–998, 2012.
- [16] S. Fujino, Y. Mizuno, K. Takaoka, J. Nakano, M. Mori, K. Maezawa, "Experimental Demonstration of Noise Shaping in the Digital Microphone Employing Frequency ΔΣ Modulation," IEICE Trans. Electron. (Japanese Edition), Vol. J96-C, No. 12, pp. 554-555, 2013.
- [17] K. Maezawa, S. Fujino, T. Yamaoka and M. Mori, "Delta Sigma Modulation Microphone Sensors Using a Microwave Cavity Resonator," Electron. Lett. 52, pp. 1651-1652, 2016. DOI: 10.1049/el.2016.2538
- [18] T. Tajika, Y. Kakutani, M. Mori, and K. Maezawa, "Experimental demonstration of strain detection using resonant tunneling deltasigma modulation sensors," Phys. Status Solidi, A 214, No. 3, 1600548, 2016. DOI: 10.1002/pssa.201600548.
- [19] K. Maezawa, T. Takumi, M. Mori, "1 MHz strain detection using resonant tunneling delta sigma modulation sensors," AWAD 2018, Kitakyushu, A6-2, 2018.
- [20] K. Maezawa, T. Ito, M. Mori, "Delta-sigma modulation microphone sensors employing a resonant tunneling diode with a suspended microstrip resonator," Sensor Review, Vol.40, No.5, pp.535-542, 2020. DOI: 10.1108/SR-03-2020-0044.
- [21] A. Hajimiri, T. H. Lee, "A General Theory of Phase Noise in Electrical Oscillators," IEEE J. Solid-State Circ., Vol. 33, pp. 179-194, 1998.
- [22] M. Odyniec, RF and microwave oscillator design, Artech House, Boston, 2002.
- [23] E. Rubiola, Phase noise and frequency stability in oscillators, Cambridge University Press, Cambridge, 2009.
- [24] S.M. Kayser Azam, Muhammad I. Ibrahimy, S.M.A. Motakabber, and A.K.M. Zakir Hossain, "Plans for Planar: Phase-Noise Reduction Techniques in Voltage-Controlled Oscillators," IEEE Microwave Mag., Vol. 20, pp. 92-108, 2019.
- [25] M. Høvin, First-order frequency Δ-Σ modulation, Ph. D. Thesis, University of Oslo, pp. 76-82, 2000.
- [26] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," Proc. IEEE, pp. 329-330, 1966.
- [27] K. Itoh, "Basis of Microwave Synthesizers [I]: Foundation of Low Noise PLL Frequency Synthesizers," J. IEICE, Vol. 88, No. 12, PP 995–1001, 2005.
- [28] K. Maezawa, M. Mori, "Effects of the Phase Noise of the Oscillators on the Frequency Delta Sigma Modulation Sensors," IEICE Technical Report, ED2019 27-32, pp. 13-16.
- [29] F. Medeiro, B. P.-Verdu and A. R.-Vazquez, *Top-down design of high-performance sigma-delta modulators*, pp. 79-80, Kluwer Academic Publishers, Boston, 1999.
- [30] K. Maezawa, T. Yamaoka, M. Mori, "A 10GS/s measurement system using an FPGA for frequency delta-sigma modulation sensors," IEICE Technical Report, ED2018-25 (2018-08), pp. 31-34.